Twelve Channel Half Bridge Drivers

GENERAL DESCRIPTION

The SiLM94112-AQ is a protected twelve-fold half-bridge driver designed especially for automotive motion control applications such as Heating, Ventilation and Air Conditioning (HVAC) flap DC motor control.

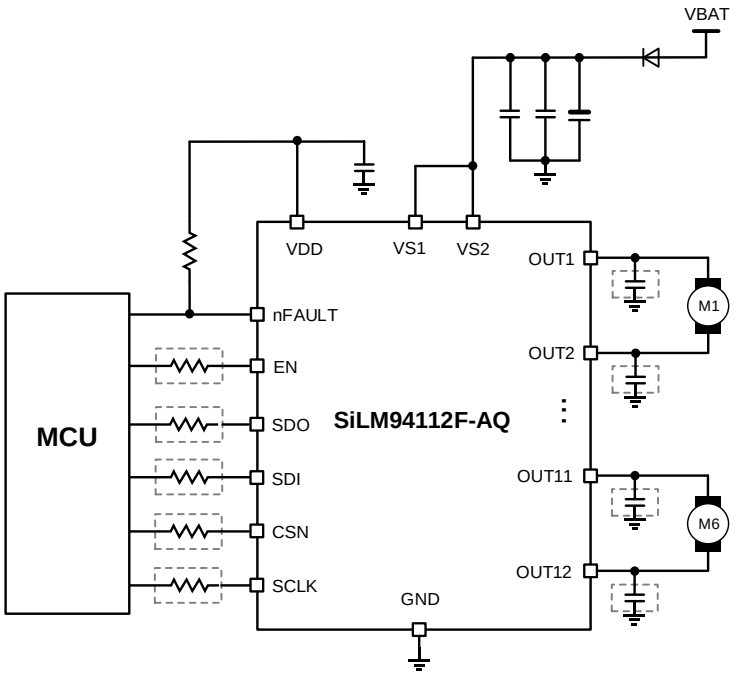
The half bridge drivers are designed to drive DC motor loads in sequential operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a 16-bit SPI interface. It offers diagnosis features such as short circuit, overcurrent, open load, power supply failure and overtemperature detection. This device is attractive for automotive applications considering its low quiescent current. The small fine pitch exposed pad package, TSSOP24-EP, provides good thermal performance and reduces PCB-board space and costs.

APPLICATIONS

- HVAC Flap DC motors
- Monostable and bistable Relays
- Side mirror x-y adjustment and mirror fold
- LEDs

FEATURES

- Twelve half bridge power outputs
- Very low power consumption in sleep mode
- 3.3V/5V compatible inputs with hysteresis
- All outputs with overload and short circuit protection
- Independently diagnosable outputs (overcurrent, open load)
- Open load diagnostics in ON-state for all high-side and low-side
- Outputs with open load thresholds
- 16-bit Standard SPI interface with daisy chain and in-frame response capability for control and diagnosis
- Fast diagnosis with the global error flag
- PWM capable outputs for frequencies 80Hz, 100Hz,200Hz and 2kHz with 8-bit duty cycle resolution
- Overtemperature pre-warning and protection
- Overvoltage and Undervoltage lockout
- Cross-current protection
- nFAULT pin indicator(Only SiLM94112F-AQ)
- AEC-Q 100 qualified for automotive



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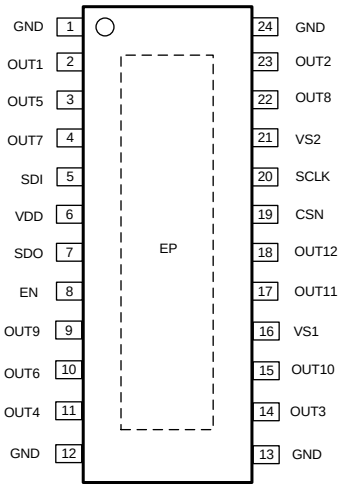
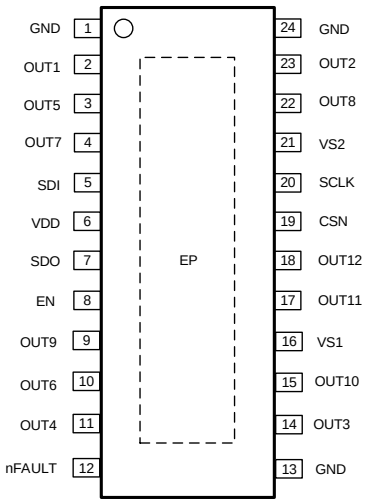
PIN CONFIGURATION

Package	Pin Configuration (Top View)	
TSSOP24-EP		
	SiLM94112MG-AQ	SiLM94112FMG-AQ

PIN DESCRIPTION

No.	Pin	Description
1	GND	Ground. All ground pins should be externally connected together.
2	OUT1	Power half-bridge 1
3	OUT5	Power half-bridge 5
4	OUT7	Power half-bridge 7
5	SDI	Serial data input with internal pull down
6	VDD	Logic supply voltage
7	SDO	Serial data output
8	EN	Enable with internal pull-down; Places device in standby mode by pulling the EN line Low
9	OUT9	Power half-bridge 9
10	OUT6	Power half-bridge 6
11	OUT4	Power half-bridge 4
12	GND	Ground. All ground pins should be externally connected together.
	nFAULT	Fault indicator output. Pulled logic low during a fault condition and requires an external pull-up resistor. (Only SiLM94112F-AQ)
13	GND	Ground. All ground pins should be externally connected together.
14	OUT3	Power half-bridge 3
15	OUT10	Power half-bridge 10

No.	Pin	Description
16	VS1	Main supply voltage for power half bridges. VS1 should be externally connected to VS2.
17	OUT11	Power half-bridge 11
18	OUT12	Power half-bridge 12
19	CSN	Chip select Not input with internal pull up
20	SCLK	Serial clock input with internal pull down
21	VS2	Main supply voltage for power half bridges. VS1 should be externally connected to VS2.
22	OUT8	Power half-bridge 8
23	OUT2	Power half-bridge 2
24	GND	Ground. All ground pins should be externally connected together.
EP	-	Exposed Die Pad; For cooling and EMC purposes only - not usable as electrical ground. Electrical ground must be provided by pins 1,12,13,24. 1)

ORDERING INFORMATION

Order Part No.	nFault Feature	Package	QTY
SiLM94112MG-AQ	No	TSSOP24-EP, Pb-Free	4000/Reel
SiLM94112FMG-AQ	Yes	TSSOP24-EP, Pb-Free	4000/Reel

FUNCTIONAL BLOCK DIAGRAM

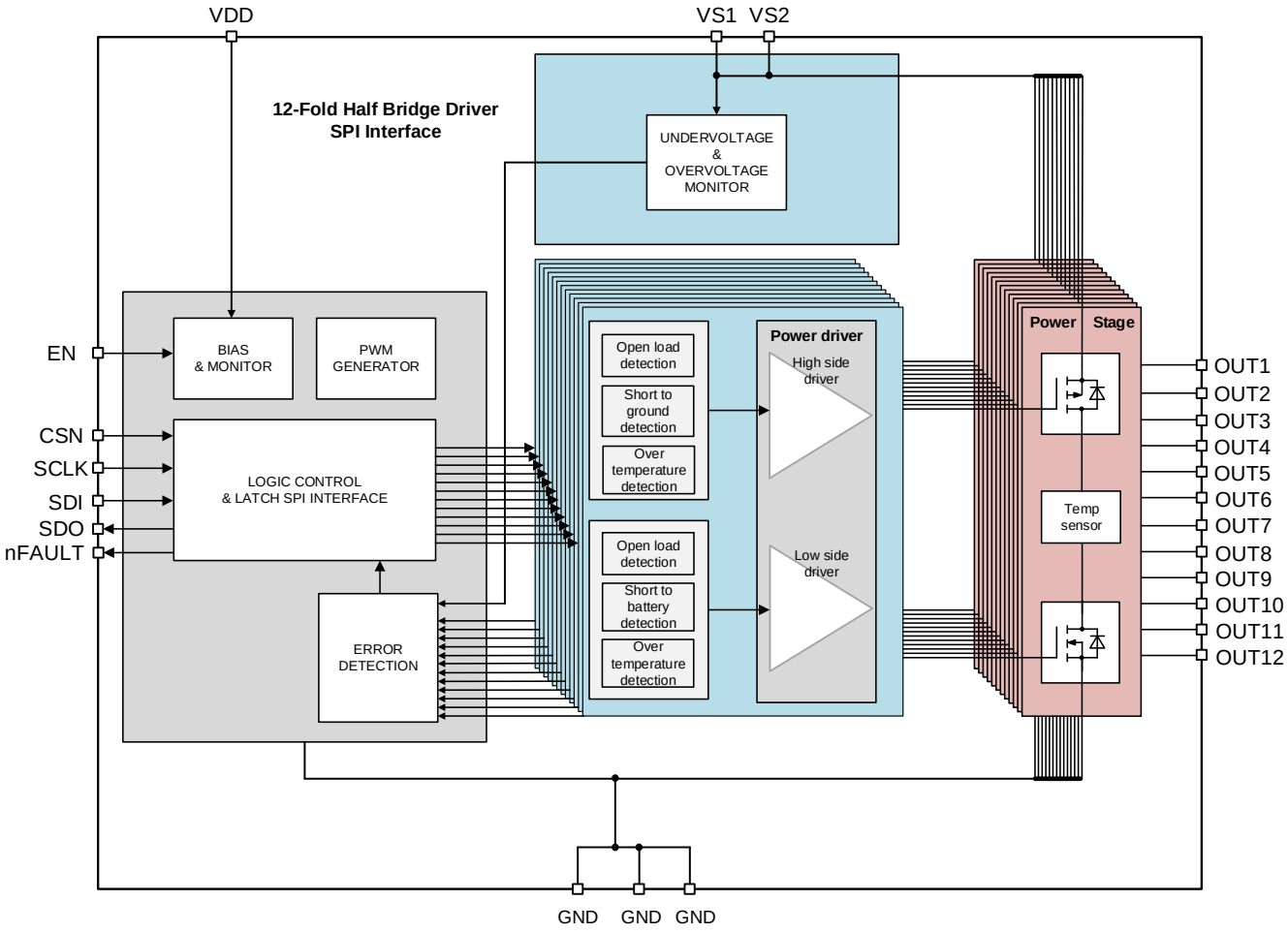


Figure 1. Block Diagram SiLM94112F-AQ (SPI Interface)

VOLTAGE AND CURRENT DEFINITION

Figure 2 shows terms used in this datasheet, with associated convention for positive values.

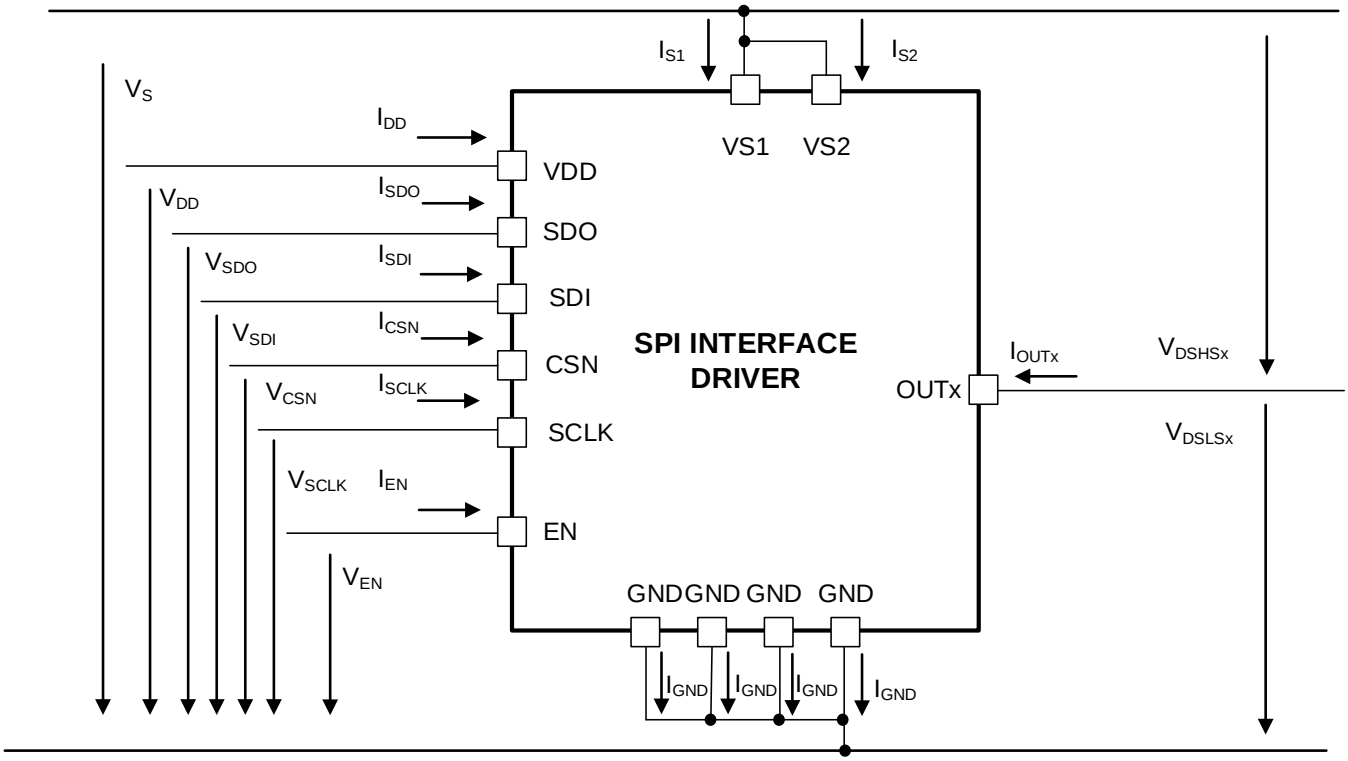


Figure 2. Voltage and current Definition

ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_S	Supply voltage	-0.3	40	V
dV_S/dt	Supply Voltage Slew Rate		10	V/us
V_{OUT}	Power half-bridge output voltage	- 0.3	40	V
V_{DD}	Logic supply voltage	-0.3	5.5	V
V_{SDI} V_{SCLK} V_{CSN} V_{EN}	Logic input voltages (SDI, SCLK, CSN, EN)	-0.3	V_{DD}	V
V_{nFAULT}, V_{SDO}	Logic output voltage (SDO, nFAULT)	-0.3	V_{DD}	V
I_{S1}	Continuous Supply Current for VS1	0	3.0	A
I_{S2}	Continuous Supply Current for VS2	0	3.0	A
I_{GND}	Current per GND pin	0	2.0	A
I_{OUT}	Output Currents	-2.0	2.0	A
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-50	150	°C
V_{ESD}	HBM	-6000	6000	V
V_{ESD}	CDM	-2000	2000	V

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min	Max	Units
$V_{S(nor)}$	Supply voltage range for normal operation	4.6	32	V
V_{DD}	Logic supply voltage range for normal operation	3.0	5.5	
V_{SDI},V_{SCLK} V_{CSN},V_{EN}	Logic input voltages (SDI, SCLK, CSN, EN)	-0.3	5.5	
T_J	Junction temperature	- 40	150	°C

THERMAL RESISTANCE

Symbol	Definition	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance[1]	31	℃/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance[1]	13	℃/W

Note1: thermal resistance is based on standard JESD51-7 high effective thermal conductivity test board

ELECTRICAML CHARACTERISTICS

V_S =4.6 V to 32 V, V_{DD} = 3.0V to 5.5V, T_J = -40 ~ 125°C, EN= HIGH, I_{OUTn}= 0A; Typical values refer to V_{DD} = 5.0 V, V_S = 13.5 V unless otherwise specified; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Current Consumption, EN=GND						
I_{SQ}	Supply Quiescent current	EN=GND	---	0.5	4	μA
I_{DD_Q}	Logic supply quiescent current		---	0.1	2	
I_{SQ}+I_{DD_Q}	Total quiescent current		---	0.6	6	
Current Consumption, EN=HIGH						
I_S	Supply current	Power drivers and power stages are off	---	0.35	0.7	mA
I_{S_HSON}[1]	Supply current	All high-sides ON	---	4	8	
I_{DD}	Logic current	SPI not active	---	0.8	1.5	
I_{DD_RUN}[2]	Logic supply current	SPI 5MHz	---	2	---	
I_S + I_{DD_RUN}[2]	Total supply current	SPI 5MHz	---	2.35	---	
Over and Undervoltage Lockout						
V_{UV_ON}	Undervoltage Switch ON voltage threshold	V_S increasing	4	4.3	4.6	V
V_{UV_OFF}	Undervoltage Switch OFF voltage threshold	V_S decreasing	3.8	4.1	4.4	
V_{UV_HY}[2]	Undervoltage Switch ON/OFF hysteresis	V_{UV_ON} - V_{UV_OFF}	---	0.2	---	
V_{OV1_OFF}	Overvoltage Switch OFF voltage threshold	V_S increasing	21	---	25	
V_{OV1_ON}	Overvoltage Switch ON voltage threshold	V_S decreasing	20	---	24	
V_{OV1_HY}[2]	Overvoltage Switch ON/OFF hysteresis	V_{OV1_OFF} – V_{OV1_ON}	---	1.0	---	
V_{OV2_OFF}	Overvoltage Switch OFF voltage threshold	V_S increasing	32.7	---	36	
V_{OV2_ON}	Overvoltage Switch ON voltage threshold	V_S decreasing	32	---	35	
V_{OV2_HY}[2]	Overvoltage Switch ON/OFF hysteresis	V_{OV2_OFF} – V_{OV2_ON}	---	1.0	---	
V_{DD_POR}	V_{DD} Power-On-Reset	V_{DD} increasing	2.4	2.7	2.9	
V_{DD_POffR}	V_{DD} Power-Off-Reset	V_{DD} decreasing	2.35	2.55	2.85	

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$V_{DD\_POR\_HY}$[2]	V_{DD} Power ON/OFF hysteresis	V_{DD_POR} - V_{DD_POffR}	---	0.15	---	
Static Drain-source On-Resistance (High-Side or Low-Side)						
$R_{DSON\_HB\_25C}$	High-Side or Low-Side RDSON (all outputs)	I_{OUT} = ±0.5 A;T_J = 25 °C	---	900	1200	mΩ
$R_{DSON\_HB\_125C}$	High-Side or Low-Side RDSON (all outputs)	I_{OUT} = ±0.5 A; T_J = 125 °C	---	1400	1800	mΩ
Output Protection and Diagnosis of high-side (HS) channels of half-bridge output						
I_{SD_HS}	HS Overcurrent Shutdown Threshold	See Figure 5	0.9	1.1	1.4	A
I_{LIM_HS}- I_{SD_HS}[2]	Difference between shutdown and limit current	$\|I_{LIM\_HS}\| \geq \|I_{SD\_HS}\|$ See Figure 5	0	0.6	1.2	A
T_{dSD_HS}[2]	Overcurrent Shutdown filter time		15	18	23	μs
I_{OLD_HS}	Open Load Detection Current		3	8	20	mA
I_{OLDN_HS}	Open Load Detection negative Current		3	8	20	mA
t_{OLD_HS}[2]	Open Load Detection filter time		2000	3000	4000	μs
Output Protection and Diagnosis of low-side (LS) channels of half-bridge output						
I_{SD_LS}	LS Overcurrent Shutdown Threshold	Figure 6	0.9	1.1	1.4	A
I_{LIM_LS}-I_{SD_LS}	Difference between shutdown and limit current	$I_{LIM\_LS} \geq I_{SD\_LS}$ Figure 6	0	0.6	1.2	A
t_{dSD_LS}[2]	Overcurrent Shutdown filter time		15	18	23	μs
I_{OLD_LS}	Open Load Detection Current		3	8	20	mA
I_{OLDN_LS}	Open Load Detection negative Current		3	8	20	mA
t_{OLD_LS}[2]	Open Load Detection filter time		2000	3000	4000	μs
Outputs OUT(1...n) leakage current						
I_{QLHn_NOR}	HS leakage current in off state	V_{OUTn} = 0V ; EN=High		0.5	2	μA
I_{QLHn_SLE}	HS leakage current in off state	V_{OUTn} = 0V ; EN=GND		0.5	2	μA
I_{QLLn_NOR}	LS leakage current in off state	V_{OUTn} = V_S ; EN=High		0.5	2	μA
I_{QLLn_SLE}	LS leakage current in off state	V_{OUTn} = V_S ; EN=GND		0.5	2	μA
Output Switching Times						
dV_{OUT}/dt[3]	Slew rate of high-side and low-side outputs	Resistive load = 100Ω; V_S=13.5V	0.1	0.35	3.5	V/ μs
t_{dONH}	Output delay time high side driver on	Resistive load = 100Ω to GND	5	20	35	μs

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{dOFFH}	Output delay time high side driver off	Resistive load = 100Ω to GND	15	45	75	µs
t_{dONL}	Output delay time low side driver on	Resistive load = 100Ω to V_S	5	20	35	µs
t_{dOFFL}	Output delay time low side driver off	Resistive load = 100Ω to V_S	15	45	75	µs
t_{DHL}[2]	Cross current protection time, high to low	Resistive load = 100Ω	100	128	160	µs
t_{DLH}[2]	Cross current protection time, low to high	Resistive load = 100Ω	100	128	160	µs
Input Interface: Logic Input EN						
V_{ENH}	High-input voltage		0.75 * V_{DD}			V
V_{ENL}	Low-input voltage				0.25 * V_{DD}	V
V_{ENHY}[2]	Hysteresis of input voltage			1700		mV
R_{PD_EN}	Pull down resistor	V_{EN} = 0.2 x V_{DD}	20	40	70	kΩ
SPI Interface						
$f_{SPI,max}$[2,4]	Maximum SPI frequency				5.0	MHz
t_{SET}[2]	Setup time	See Figure 12			150	µs
V_{IH}	H-input voltage threshold		0.7 * V_{DD}			V
V_{IL}	L-input voltage threshold				0.3 * V_{DD}	V
V_{HY}[2]	Hysteresis of input voltage			500		mV
R_{PU_CSN}	Pull up resistor at pin CSN	V_{CSN} = 0.7 x VDD	30	50	80	kΩ
R_{PD_SDI}, R_{PD_SCLK}	Pull down resistor at pin SDI, SCLK	V_{SDI}, V_{SCLK} = 0.2 x V_{DD}	20	40	70	kΩ
C_I[2]	Input capacitance at pin CSN, SDI or SCLK	0V < V_{DD} < 5.25V		10	15	pF
V_{SDOH}, $V_{nFAULTH}$	H-output voltage level	I_{SDOH} = -1.6 mA	V_{DD} - 0.4	V_{DD} - 0.2		V
V_{SDOL}, $V_{nFAULTL}$	L-output voltage level	I_{SDOL} = 1.6 mA		0.2	0.4	V
I_{SDOLK}, $V_{nFAULTLK}$	Tri-state Leakage Current	V_{CSN} = V_{DD}; 0V < V_{SDO} < V_{DD}	-1		1	µA
C_{SDO}[2]	Tri-state input capacitance			10	15	pF
Data Input Timing[2]						
t_{pCLK}	SCLK Period		200			ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{SCLKH}	SCLK High Time		0.45 * t_{pCLK}		0.55 * t_{pCLK}	ns
t_{SCLKL}	SCLK Low Time		0.45 * t_{pCLK}		0.55 * t_{pCLK}	ns
t_{BEF}	SCLK Low before CSN Low		125			ns
t_{lead}	CSN Setup Time		250			ns
t_{lag}	SCLK Setup Time		250			ns
t_{BEH}	SCLK Low after CSN High		125			ns
t_{SDI_setup}	SDI Setup Time		30			ns
t_{SDI_hold}	SDI Hold Time		30			ns
t_{rIN}	Input Signal Rise Time at pin SDI, SCLK, CSN				50	ns
t_{fIN}	Input Signal Fall Time at pin SDI, SCLK, CSN				50	ns
t_{DMODE}	Delay time from EN falling edge to standby mode				8	μs
t_{CSNH}	Minimum CSN High Time		5			μs
Data Output Timing[2]						
t_{rSDO}	SDO Rise Time	C_{load} = 40pF		30	80	ns
t_{fSDO}	SDO Fall Time	C_{load} = 40pF		30	80	ns
t_{ENSDO}	SDO Enable Time after CSN falling edge	Low Impedance			75	ns
t_{DISSDO}	SDO Disable Time after CSN rising edge	High Impedance			75	ns
$duty_{SCLK}$	Duty cycle of incoming clock at SCLK		45		55	%
t_{VASDO3}	SDO Valid Time for V_{DD}=3.3V	V_{SDO} < 0.2 x V_{DD} V_{SDO} > 0.8 x V_{DD} C_{load} = 40pF		70	95	ns
t_{VASDO5}	SDO Valid Time for V_{DD}=5V	V_{SDO} < 0.2 x V_{DD} V_{SDO} > 0.8 V_{DD} C_{load} = 40pF		50	65	ns
Thermal warning & Shutdown[2]						
T_{JW}	Thermal warning junction temperature	Figure 9	120	140	170	℃
T_{JSD}	Thermal shutdown junction temperature	Figure 9	150	175	200	℃
T_{JHYS}	Thermal comparator hysteresis			5		℃
T_{JSD} / T_{JW}	Ratio of SD to W temperature		1.05	1.2		

1 I_{S_HSON} does not include the load current

2 Not subject to production test, specified by design

3 Measured for 20%−80% of V_S.

4 Not applicable in daisy chain configuration

GENERAL DESCRIPTION

Power Supply

The SiLM94112-AQ has two power supply inputs, V_S and V_{DD}. The half bridge outputs are supplied by V_S, which is connected to the 12V or 24V automotive supply rail. V_{DD} is used to supply the I/O buffers and internal voltage regulator of the device.

V_S and V_{DD} supplies are separated so that information stored in the logic block remains intact in the event of voltage drop outs or disturbances on V_S. The system can therefore continue to operate once V_S has recovered, without having to resend commands to the device.

A rising edge on V_{DD} crossing V_{DD_POR} triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched off (high impedance).

An electrolytic and 100nF ceramic capacitors are recommended to be placed as close as possible to the V_S supply pin of the device for improved EMC performance in the high and low frequency band. The electrolytic capacitor must be dimensioned to prevent the V_S voltage from exceeding the absolute maximum rating. In addition, decoupling capacitors are recommended on the V_{DD} supply pin.

Operation Modes

The SiLM94112-AQ has two operations modes: Normal mode, Sleep mode.

The SiLM94112-AQ enters normal mode by setting the EN input High. In normal mode, all output transistors can be configured via SPI.

The SiLM94112-AQ enters sleep mode by setting the EN input Low. The EN input has an internal pull-down resistor.

In sleep mode, all output transistors are turned off and the SPI register banks are reset. The current consumption is reduced to I_{SQ}+I_{DD_Q}.

Reset Behavior

There are two events that will reset the SiLM94112-AQ.

If V_{DD} is below the undervoltage threshold, V_{DD_POffR}, the SPI Interface shall not function. The digital block will be deactivated, the logic contents cleared and the output stages are switched off. The digital block is initialized once V_{DD} voltage levels is above the undervoltage threshold, V_{DD_POR}. Then the NPOR bit is reset (NPOR=0 in SYS_DIAG1 and Global Status Register).

If the EN pin is pulled Low, the logic content is reset and the device enters sleep mode. The reset event is reported by the NPOR bit (NPOR=0) once the SiLM94112-AQ is in normal mode (EN=High; V_{DD} >V_{DD_POR}).

Reverse Polarity Protection

The SiLM94112-AQ requires an external reverse polarity protection. During reverse polarity, the free-wheeling diodes across the half bridge output will begin to conduct, causing an undesired current flow (I_{RB}) from ground potential to battery and excessive power dissipation across the diodes. As such, a reverse polarity protection diode is recommended.

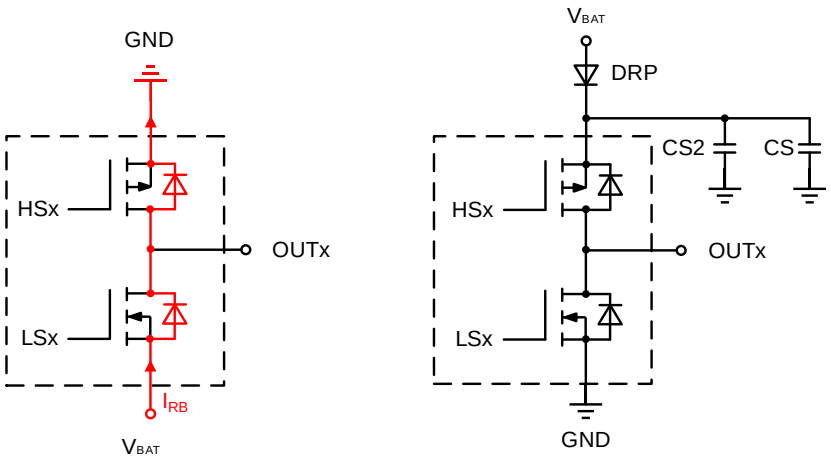


Figure 3. Reverse Polarity Protection

HALF-BRIDGE OUTPUTS

The half-bridge outputs of the SiLM94112-AQ are intended to drive motor loads. These outputs can either be driven continuously or PWM enabled via SPI.

Half-bridge Operation with Continuous Mode

If the outputs are driven continuously via SPI, for example HS1 and LS2 used to drive a motor, then the following suggested SPI commands shall be sent:

- Activate HS1: Bit HB1_HS_EN in HB_ACT_1_CTRL register
- Activate LS2: Bit HB2_LS_EN in HB_ACT_1_CTRL register

Half-bridge Operation with PWM Enabled

All half-bridge outputs of the SiLM94112-AQ are capable of PWM operation. They can either be used to drive an inductive load (e.g. DC brush motor) or optionally a resistive load (e.g. LED). Each half-bridge output has been allocated a maximum of three PWM channels with individual duty cycle settings with 8-bit resolution. Each channel is further mapped to a maximum of four PWM frequency options, i.e. 80Hz,100Hz,200Hz and 2kHz. This feature enables a highly flexible PWM operation while driving loads with varying control profiles.

PWM frequency and duty cycle can be changed on demand during PWM operation of the desired half-bridge output. Glitches on the PWM output waveform, which may arise as a result of on-demand changes in PWM operation, will be prevented by the internal logic circuitry.

When operating with motor loads, active free-wheeling configuration is available via SPI.

Note: Active free-wheeling is effectively applied if the selected duty cycle corresponds to turn-on times of the HS and the LS, which are longer than the sum of the cross conduction times t_{DHL} + t_{DLH}.

Table 1. PWM capability and frequency selection per half-bridge output

Control Register: HBx_MODEn (n=0,1)	**PWM Frequency 80Hz (Control Register: PWM_CH_FREQ_CTRL)**	**PWM Frequency 100Hz (Control Register: PWM_CH_FREQ_CTRL)**	**PWM Frequency 200Hz (Control Register: PWM_CH_FREQ_CTRL)**	**PWM Frequency 2000Hz (Control Register: OVP2_2k_CTRL)**
PWM Channel 1	PWM_CH1_FREQ_n (n=0,1) Bit ‘01B’	PWM_CH1_FREQ_n (n=0,1) Bit ‘10B’	PWM_CH1_FREQ_n (n=0,1) Bit ‘11B’	PWM_CH1_2k Bit ‘1B’
PWM Channel 2	PWM_CH2_FREQ_n (n=0,1) Bit ‘01B’	PWM_CH2_FREQ_n (n=0,1) Bit ‘10B’	PWM_CH2_FREQ_n (n=0,1) Bit ‘11B’	PWM_CH2_2k Bit ‘1B’
PWM Channel 3	PWM_CH3_FREQ_n (n=0,1) Bit ‘01B’	PWM_CH3_FREQ_n (n=0,1) Bit ‘10B’	PWM_CH3_FREQ_n (n=0,1) Bit ‘11B’	PWM_CH3_2k Bit ‘1B’

Inductive Load

Figure 4 shows an application with OUT1 and OUT2 driving a DC brush motor. With this configuration, HS1 is permanently driven while LS2 is driven in PWM operation. HS2 serves to actively free-wheel (FW) the motor current load, reducing the power dissipation of the device.

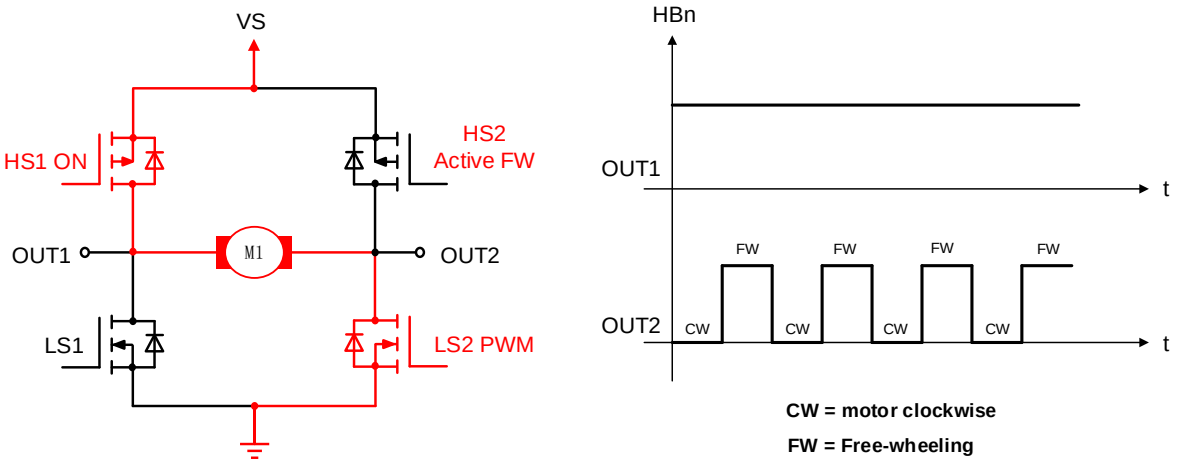


Figure 4. PWM operation on OUT 2

Assuming HBx Mode=00 and both HSx and LSx are considered off (tri-state). The suggested SPI control commands for proper PWM operation are:

- Configure the frequency to 00 (PWM is stopped and off) for selected PWM channel
- Assign an appropriate PWM channel for selected half-bridge output in HB_MODE_CTRL register
- Configure the duty cycle of the selected half-bridge output in PWM_DC_CTRL register
- Select the PWM frequency in PWM_CH_FREQ_CTRL or OVP2_2k_CTRL register to begin the PWM period
- Activate the channel to be driven in PWM operation: HSn or LSn in the HB_ACT_CTRL register

Careful attention should be paid to the free-wheeling configuration of the half-bridge required to be driven in PWM operation. For example, in the event a high-side channel is activated and assigned a PWM channel, and active free-wheeling is selected, but a frequency mode of '00' (PWM is stopped and off) is configured in the PWM_CH_FREQ_CTRL register, then the respective high-side channel will be configured low and the adjacent low-side channel within the half-bridge will be enabled. This is a result of enabling active free-wheeling.

Protection and Diagnosis

The SiLM94112-AQ is equipped with an SPI interface to control and diagnose the state of the half-bridge drivers. This device has embedded protective functions which are designed to prevent IC destruction under fault conditions described in the following sections. Fault conditions are treated as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation. Once the fault occur, the nFAULT pin is pull low(Only SiLM94112F).

The following table provides a summary of fault conditions, protection mechanisms and recovery states embedded in the SiLM94112-AQ device.

Table 2. Summary of diagnosis and monitoring of outputs

Fault Condition	Error Flag (EF) Behaviour	Error Bit: Status Register	Output Protection Mechanism	Output Error State	nFAULT pin	Output and Error Flag (EF) Recovery
Overcurrent	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OC and HBn_LS_OC bits in SYS_DIAG_2, SYS_DIAG_3, SYS_DIAG_4 status registers	Error output shutdown and latched	High-Z	Low	Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage.
Open load	Latch	1. Load Error bit, LE (bit 6) in SYS_DIAG 1: Global Status 1 Register 2. Localized error for each HS and LS channel of half-bridge, HBn_HS_OL and HBn_LS_OL bits in SYS_DIAG_5, SYS_DIAG_6, SYS_DIAG_7 status registers	None	No state change	Low	An open load detection does not change the state of the output. EF to be cleared.
Temperature pre-warning	Latch	Global error bit 1, TPW in SYS_DIAG_1: Global Status 1 register	None	No state change	Low	Not applicable
Temperature shutdown	Latch	Global error bit 2, TSD in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and latched.	High-Z	Low	Half-bridge control bits remain set despite error, however the output stage is shutdown. Clear EF to reactivate output stage.
Power supply failure due to undervoltage	Latch	Global error bit 5, VS_UV in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and automatically recovers.	High-Z	Low	Half-bridge control bits remain set despite error, however the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared.
Power supply failure due to overvoltage	Latch	Global error bit 4, VS_OV in SYS_DIAG_1: Global Status 1 register	All outputs shutdown and automatically recover	High-Z	Low	Half-bridge control bits remain set despite error, however the output stage is shutdown. They will automatically be reactivated once the power supply recovers. EF to be cleared.

Short Circuit of Output to Supply or Ground

The high-side switches are protected against short to ground whereas the low-side switches are protected against short to supply.

The high-side and low-side power switches will enter into an over-current condition if the current within the switch exceeds the overcurrent shutdown detection threshold, I_{SD}. Upon detection of the I_{SD} threshold, an overcurrent shutdown filter, t_{dSD} is begun. As the current rises beyond the threshold I_{SD}, it will be limited by the current limit threshold, I_{LIM}. Upon expiry of the overcurrent shutdown filter time, the affected power switch is latched off and the corresponding error bit, HBn_HS_OC or HBn_LS_OC is set and latched. See Figure 5 and Figure 6 for more detail.

A global load error bit, LE, contained in the global status register, SYS_DIAG_1, is also set for ease of error scanning by the application software. The power switch remains deactivated as long as the error bit is set.

To resume normal functionality of the power switch (in the event the overcurrent condition disappears or to verify if the failure still exists) the microcontroller shall clear the error bit in the respective status register to reactivate the desired power switch.

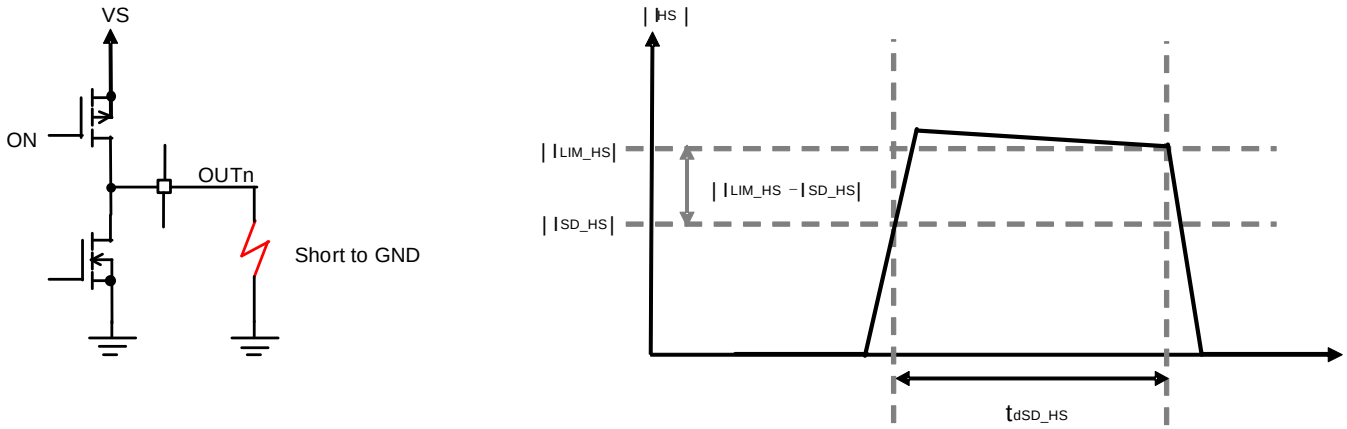


Figure 5. High-Side Switch - Short Circuit and Overcurrent Protection

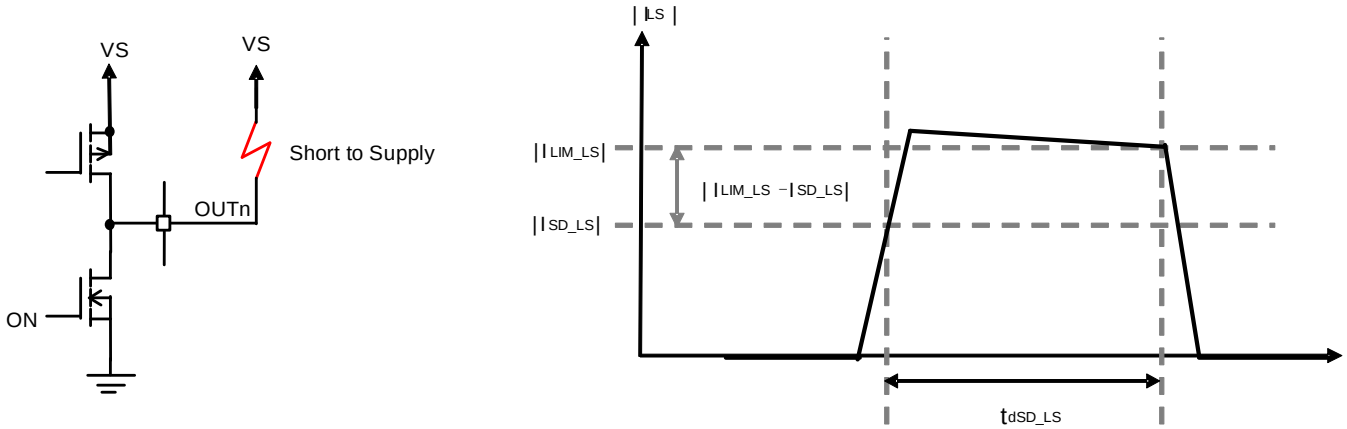


Figure 6. Low-Side Switch - Short Circuit and Overcurrent Protection

Table 3. Control and Status register bit state in the event of an overcurrent condition for an activated power switch

Register Type	Register Name	Bit Name	Before Overcurrent	During Overcurrent	After Overcurrent
			Bit State	Bit State	Bit State
Control	HB_ACT_CTRL_n	HBn_HS_EN HBn_LS_EN	1	1	1 (corresponding half-bridge deactivated)
Status	SYS_DIAG_1: Global Status 1	LE	0	0	1
Status	SYS_DIAG_x where x=2,3,4	HBn_HS_OC HBn_LS_OC	0	0	1

Cross-Current

In bridge configurations the high-side and low-side power transistors are ensured never to be simultaneously “ON” to avoid cross currents. This is achieved by integrating delays in the driver stage of the power outputs to create a dead-time between switching off of one power transistor and switching on of the adjacent power transistor within the half-bridge. The dead times, t_{DHL} and t_{DLH}, as shown in Figure 7 case 3 and Figure 8 case 3, have been specified to ensure that the switching slopes do not overlap with each other. This prevents a cross conduction event.

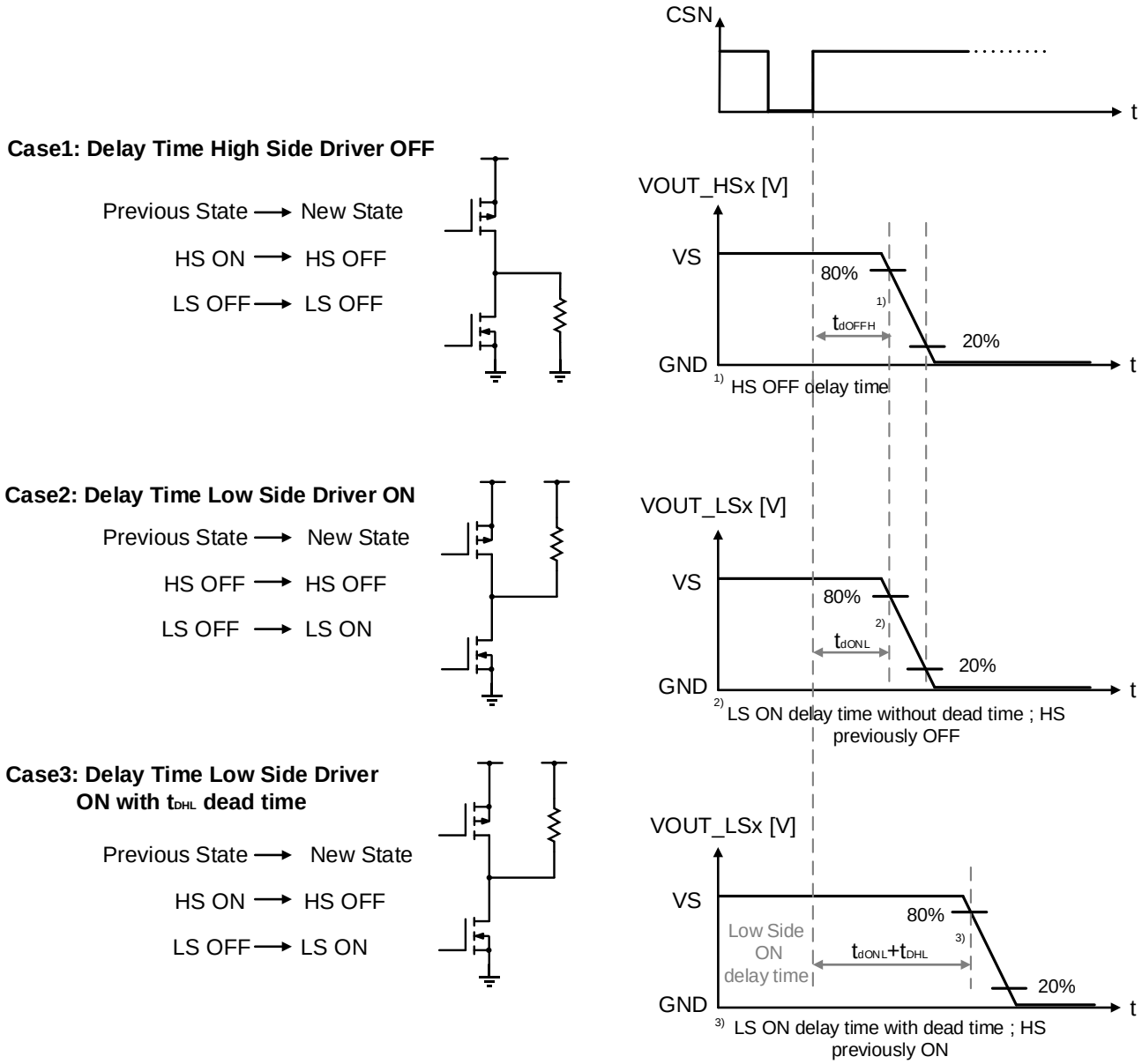


Figure 7. Half bridge outputs switching times - high-side to low-side transition

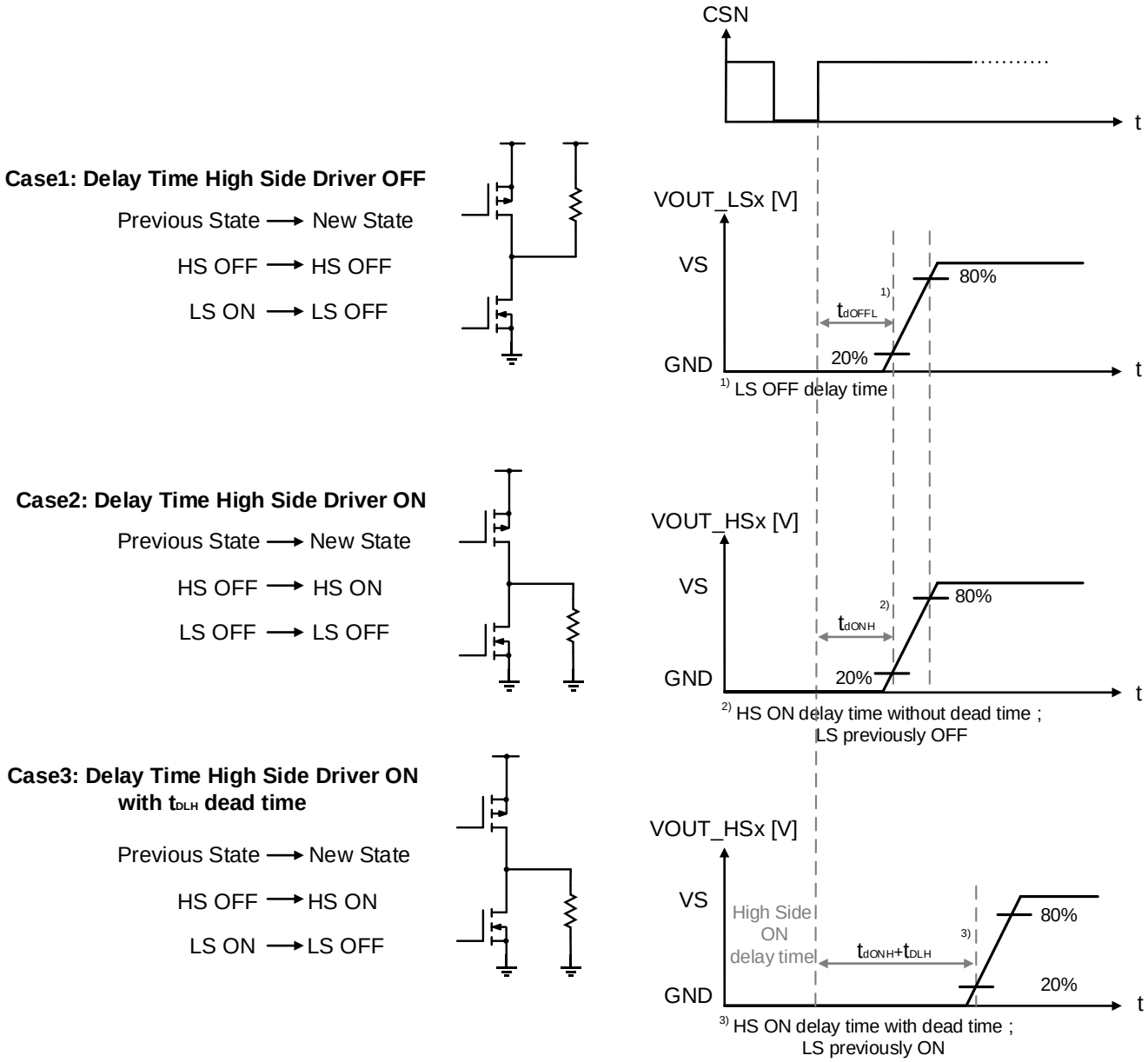


Figure 8. Half bridge outputs switching times- low-side to high-side transition

Temperature Monitoring

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If one or more temperature sensors reach the warning temperature, the temperature pre-warning bit, TPW is set. This bit is latched and can only be cleared via SPI. The outputs stages however remain activated.

If one or more temperature sensors reach the shut-down temperature threshold, all outputs are latched off. The TSD bit in SYS_DIAG_1: Global Status 1 is set. All outputs remain deactivated until the TSD bit is cleared. See Figure 9.

To resume normal functionality of the power switch (in the event the overtemperature condition disappears, or to verify if the failure still exists) the microcontroller shall clear the TSD error bit in the status register to reactivate the respective power switch.

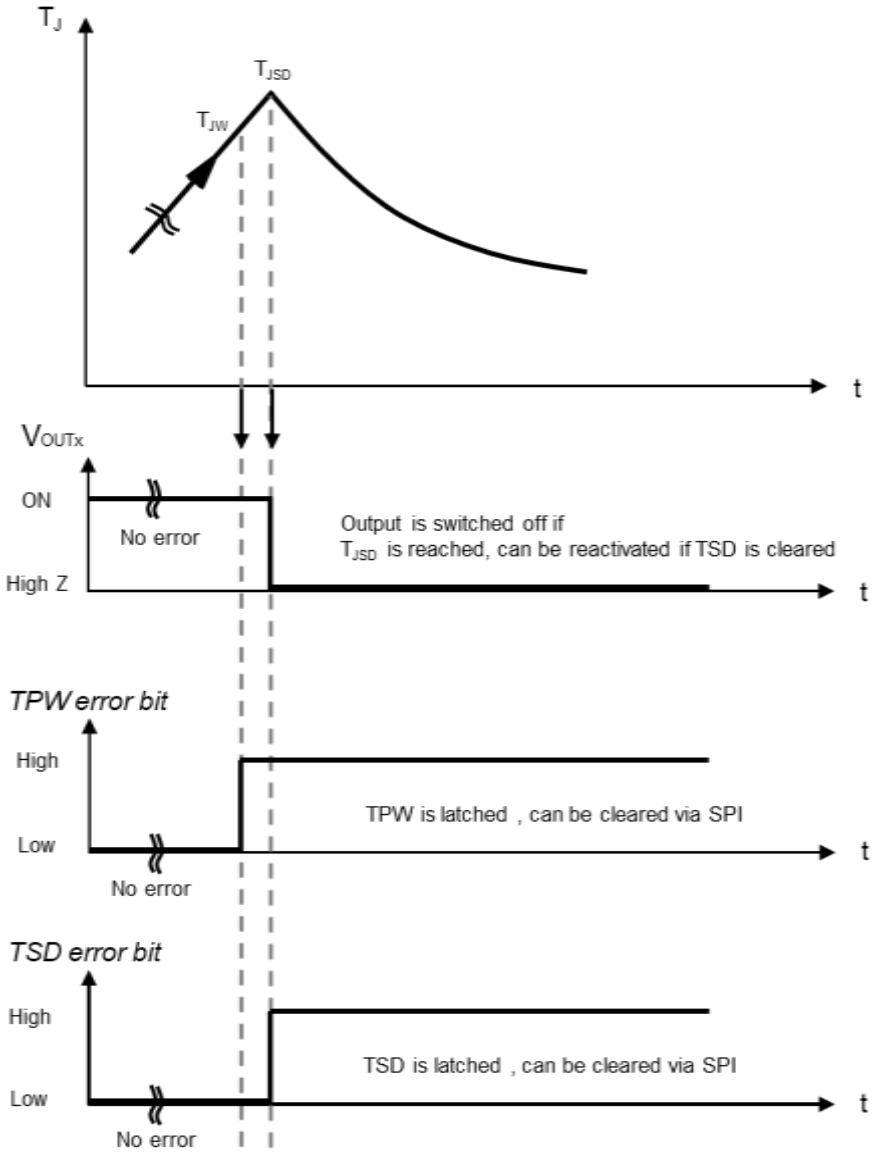


Figure 9. Overtemperature Behavior

Table 4. Control and Status register bit state in overtemperature condition for an activated power switch

Register Type	Register Name	Bit Name	$T_J<T_{JW}$	$T_J>T_{JW}$	$T_J>T_{JSD}$	$T_J<T_{JSD}-T_{JHYS}$
			Bit State	Bit State	Bit State	Bit State
Control	HB_ACT_CTRL_n	HBn_HS_EN HBn_LS_EN	1	1	1(all outputs are latched off)	'1' (outputs are latched off unless error is cleared)
Status	SYS_DIAG_1: Global status 1	TPW	0	1 (latched)	1 (latched)	'0' if error is cleared and $T_J < T_{JW}$, else '1'
Status	SYS_DIAG_1: Global status 1	TPD	0	0	1 (latched)	'0' if error is cleared, else '1'

Overvoltage and Undervoltage Shutdown

The power supply rails V_S and V_{DD} are monitored for supply fluctuations. The V_S supply is monitored for under- and over-voltage conditions where as the V_{DD} supply is monitored for under-voltage conditions.

In the event the supply voltage V_S drops below the switch off voltage V_{UV_OFF}, all output stages are switched off, however, the logic information remains intact and uncorrupted. The V_S under-voltage error bit, VS_UV, located in SYS_DIAG_1: Global Status 1 status register, will be set and latched. If VS rises again and reaches the switch on voltage V_{UV_ON} threshold, the power stages will automatically be activated. The VS_UV error bit should be cleared to verify if the supply disruption is still present. See Figure 10.

In the event the supply voltage V_S rises above the switch off voltage V_{OV1_OFF}, all output stages are switched off, The V_S over-voltage error bit, VS_OV, located in SYS_DIAG_1: Global Status 1 status register, will be set and latched. If V_S falls again and reaches the switch on voltage V_{OV1_ON} threshold, the power stages will automatically be activated. If the EXT_OVP bit in OVP2_2k_CTRL register is set, the above supply voltage V_S Threshold voltage will be V_{OV2_OFF} and V_{OV2_ON}. The VS_OV error bit should be cleared to verify if the overvoltage condition is still present. See Figure 10.

In the event the V_{DD} logic supply decreases below the undervoltage threshold, V_{DD_POffR}, the SPI interface shall no longer be functional and the SiLM94112-AQ will enter reset.

The digital block will be initialized and the output stages are switched off to High impedance. The undervoltage reset is released once V_{DD} voltage levels are above the undervoltage threshold, V_{DD_POR}.

The reset event is reported in SYS_DIAG1 by the NPOR bit (NPOR = 0) once the SiLM94112-AQ is in normal mode (EN = High; $V_{DD} > V_{DD\_POR}$).

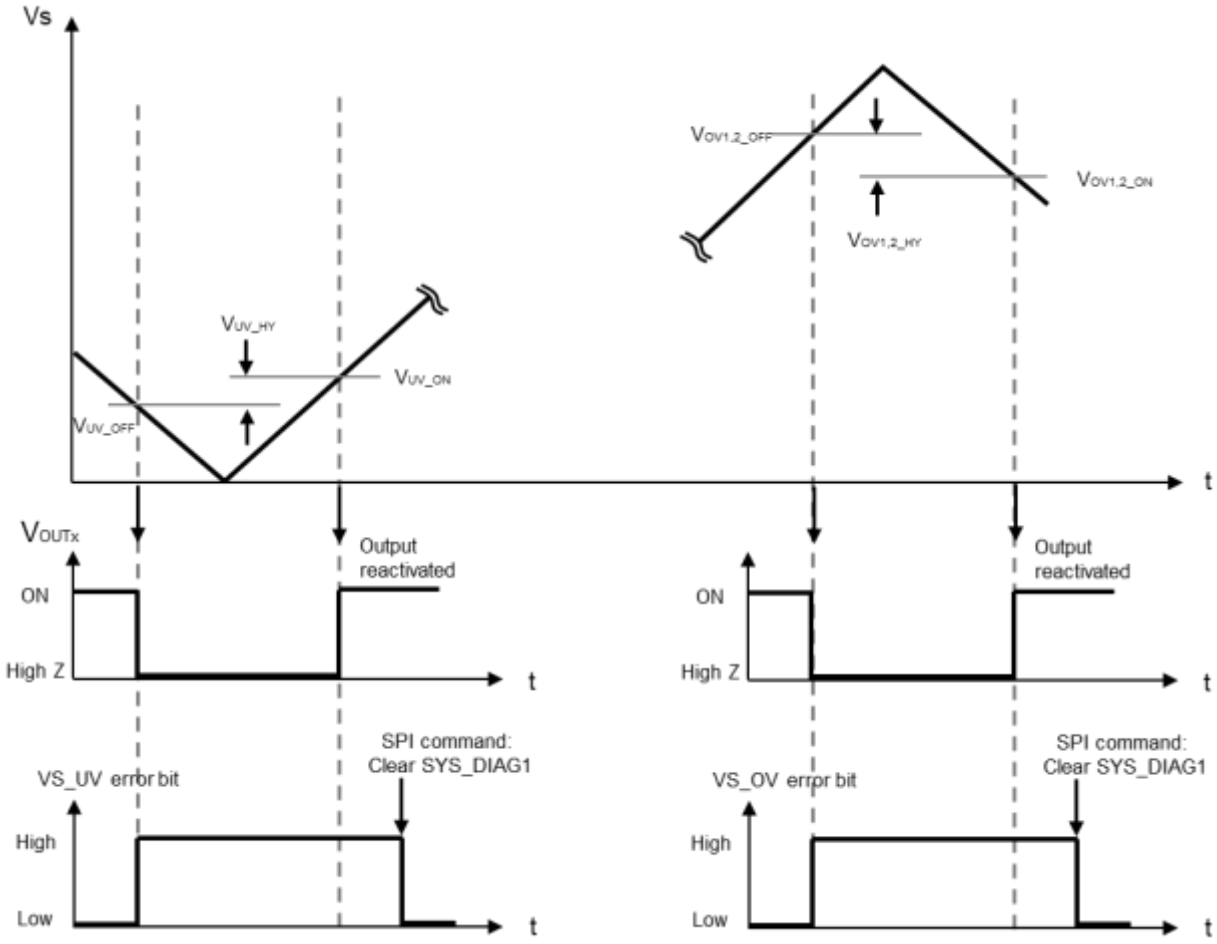


Figure 10. Output behavior during under- and overvoltage Vs condition

Open Load

Both high-side and low-side switches of the half-bridge power outputs are capable of detecting an open load in their activated state. If a load current lower than the open load detection threshold, I_{OLD} for at least t_{OLD} is detected at the activated switch, the corresponding error bit, HBn_HS_OL or HBn_LS_OL is set and latched.

A global load error bit, LE, in the global status register, SYS_DIAG_1: Global Status 1, is also set for ease of error scanning by the application software. The half-bridge output however, remains activated.

The microcontroller must clear the error bit in the respective status register to determine if the open load is still present or disappeared.

The SiLM94112-AQ device also includes a negative-current OLD mode for power stages used in active free-wheeling. The negative current can flow either through the body diode of FET or the FET itself depending on whether or not the channel is configured for synchronous rectification. The open load detection of free-wheeling FET in active mode is eliminated by enabling the Active Free Wheeling OLD setting (DIS_OL_NEG = 1 in OLDN_DT_SR_CTRL register).

SERIAL PERIPHERAL INTERFACE (SPI)

The SiLM94112-AQ has a 16-bit SPI interface for output control and diagnostics. This section describes the SPI protocol, the control and status registers.

SPI Description

The 16-bit wide Control Input Word is read via the data input SDI, which is synchronized with the clock input SCLK provided by the microcontroller. SCLK must be Low during CSN falling edge (Clock Polarity = 0). The SPI incorporates an in-frame response: the content of the addressed register is shifted out at SDO within the same SPI frame (see Figure 17 and Figure 19).The transmission cycle begins when the chip is selected by the input CSN (Chip Select Not), Low active. After the CSN input returns from Low to High, the word that has been read is interpreted according to the content. The SDO output switches to tri-state status (High impedance) at this point, thereby releasing the SDO bus for other use. The state of SDI is shifted into the input register with every falling edge on SCLK. The state of SDO is shifted out of the output register at every rising edge on SCLK (Clock Phase = 1). The SPI protocol of the SiLM94112-AQ is compatible with independent slave configuration and with daisy chain. Daisy chaining is applicable to SPI devices with the same protocol.

Writing, clearing reading is done byte wise. The SPI configuration and status bits are not cleared automatically by the device and therefore must be cleared by the microcontroller, e.g. if the TSD bit was set due to over temperature (refer to the respective register description for detailed information).

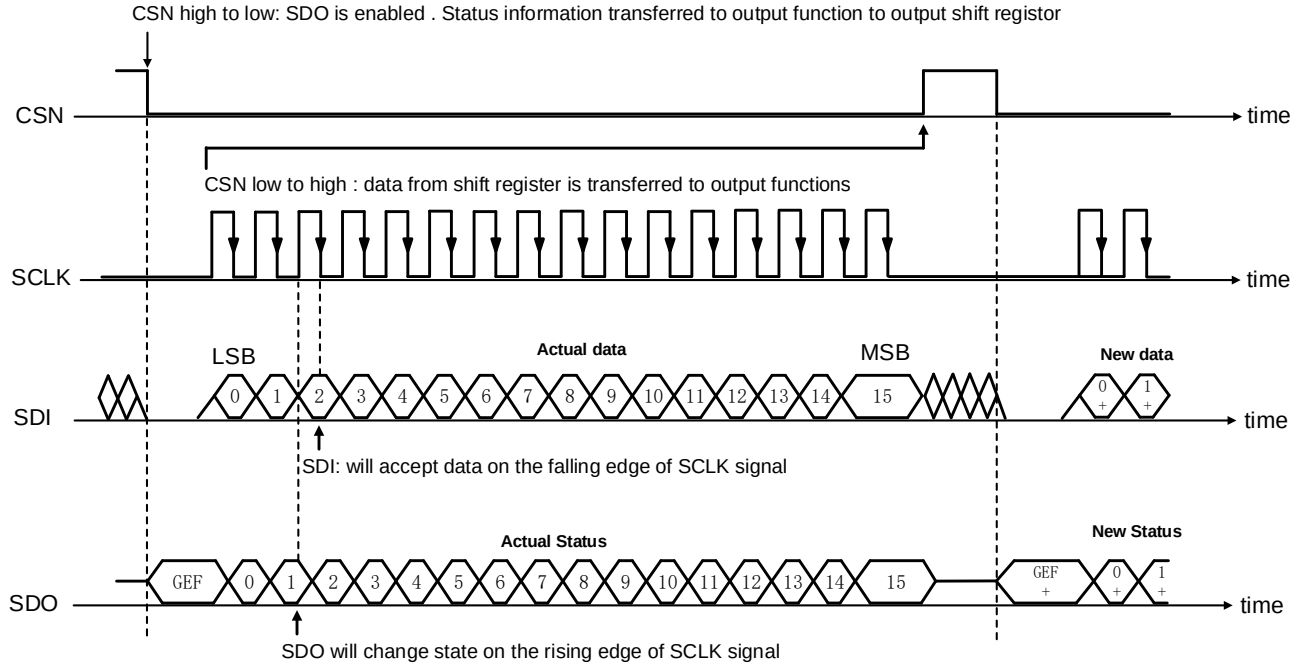


Figure 11. SPI Data Transfer Timing

SPI messages are only recognized if a minimum set time, t_{SET}, is observed upon rising edge of the EN pin (Figure 12).

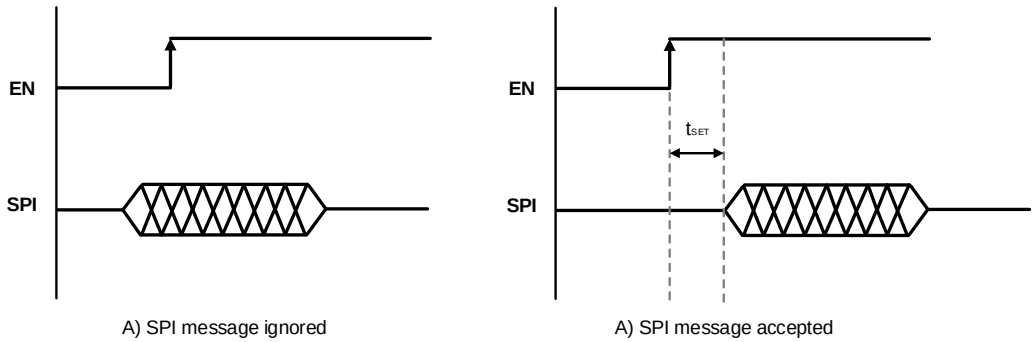


Figure 12. Setup time from EN rising edge to first SPI communication

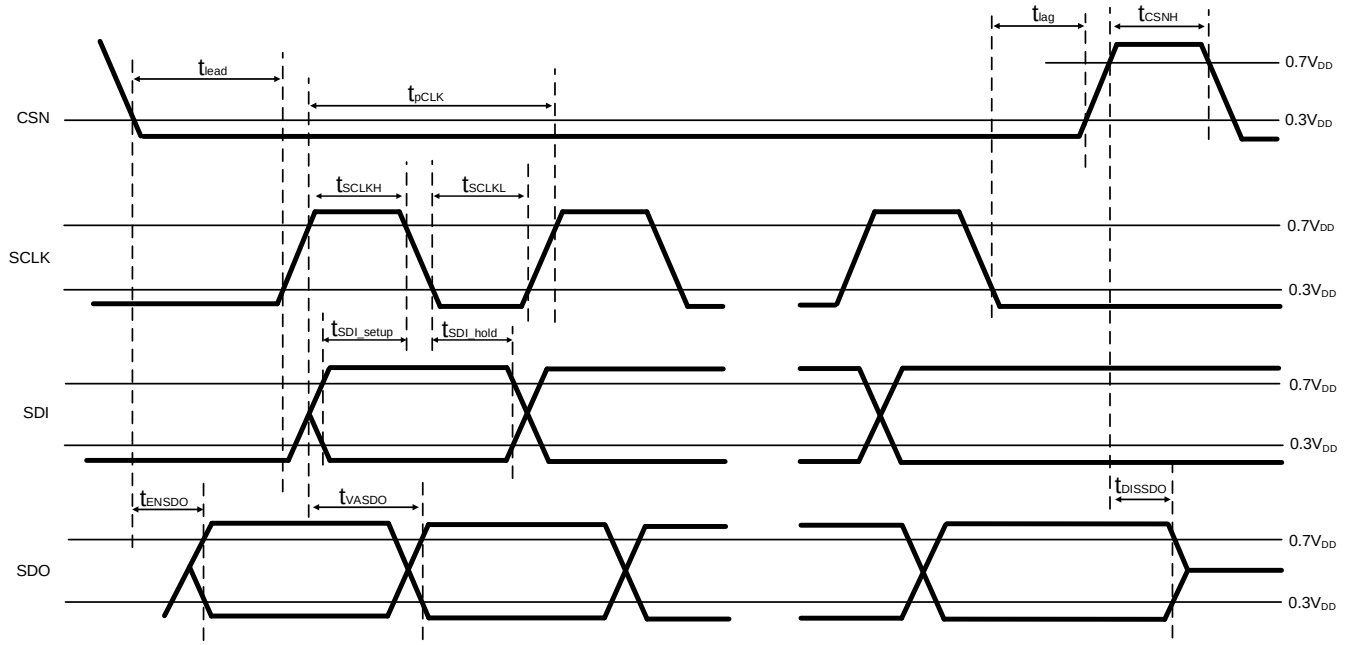


Figure 13. SPI Data Timing

Global Error Flag

A logic OR combination between Global Error Flag (GEF) and the signal present on SDI is reported on SDO between a CSN falling edge and the first SCLK rising edge (Figure 11). GEF is set if a fault condition is detected or if the device comes from a Power On Reset (POR).

Note: The SDI pin of all devices in daisy chain or non-daisy chain mode must be Low at the beginning of the SPI frame (between the CSN falling edge and the first SCLK rising edge).

It is possible to check if the SiLM94112-AQ has detected a fault by reading the GEF without SPI clock pulse (Figure 14).

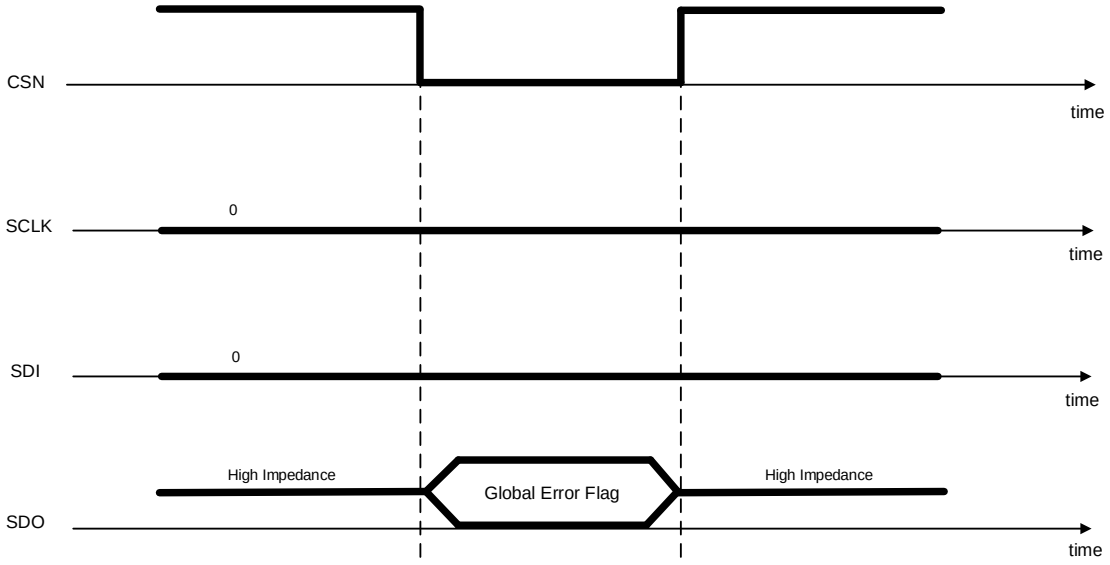


Figure 14. SDO behaviour with 0-clock cycle

Global Status Register

The SDO shifts out during the first eight SCLK cycles the Global Status Register. This register provides an overview of the device status. All failures conditions are reported in this byte:

• SPI protocol error (SPI_ERR)

• Load Error (LE bit): logical OR between Open Load (OL) and Overcurrent (OC) failures

• VS Undervoltage (VS_UV bit)

• VS Overvoltage (VS_OV bit)

• Negated Power ON Reset (NPOR bit)

• Temperature Shutdown (TSD bit)

• Temperature Pre-Warning (TPW bit)

Note: The Global Error Flag is a logic OR combination of every bit of the Global Status Register with the exception of NPOR: GEF = (SPI_ERR) OR (LE) OR (VS_UV) OR (VS_OV) OR (NOT(NPOR)) OR (TSD) OR (TPW).

The following table shows how failures are reported in the Global Status Register and by the Global Error Flag.

Table 5. Failure reported in the Global Status Register and Global Error Flag

Type of Error	**Failure reported in the Global Status Register**	**Global Error Flag**
SPI protocol error	SPI_ERR = 1	1
Open load or Overcurrent	LE = 1	1
VS Undervoltage	VS_UV = 1	1
VS Overvoltage	VS_OV = 1	1
Power ON Reset	NPOR = 0	1
Thermal Shutdown	TSD = 1	1
Thermal Warning	TPW = 1	1
No Error and no Power ON Reset	SPI_ERR = 0 LE = 0 VS_UV = 0 VS_OV = 0 NPOR = 1 TSD = 0 TPW = 0	0

Note: The default value (after Power ON Reset) of NPOR is 0, therefore the default value of GEF is 1.

SPI Protocol Error Detection

The SPI incorporates an error flag in the Global Status Register (SPI_ERR, Bit7) to supervise and preserve the data integrity. If an SPI protocol error is detected during a given frame, the SPI_ERR bit is set in the next SPI communication.

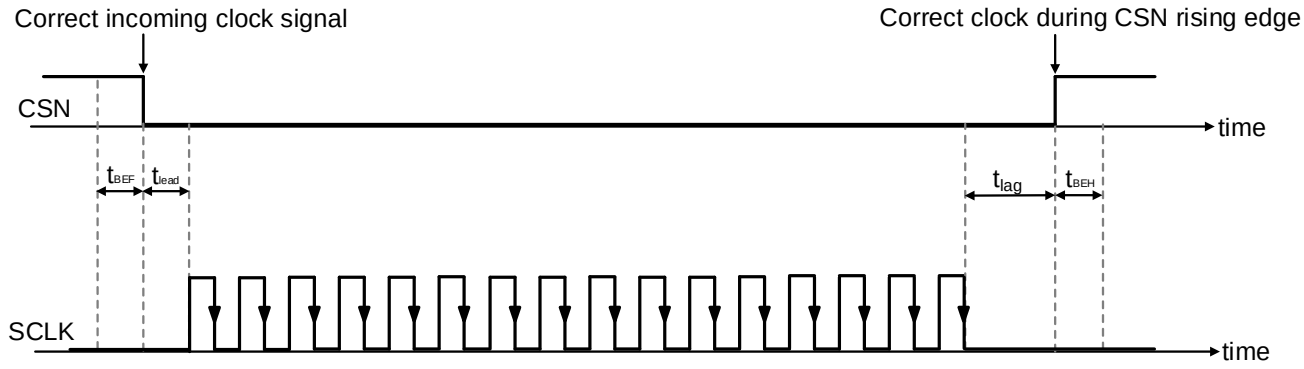
The SPI_ERR bit is set in the following error conditions:

- the number of SCLK clock pulses received when CSN is Low is not 0, or is not a multiple of 8 and at least 16
- the microcontroller sends an SPI command to an unused address. In particular, SDI stuck to High is reported in the SPI_ERR bit
- the LSB of an address byte is not set to 1. In particular, SDI stuck to Low is reported in the SPI_ERR bit
- the Last Address Bit Token (LABT, bit 1 of the address byte) in independent slave configuration is not set to 1
- the LABT bit of the last address byte in daisy chain configuration is not set to 1
- a clock polarity error is detected (see Figure 15 Case 2 and Case 3): the incoming clock signal was High during CSN rising or falling edges.

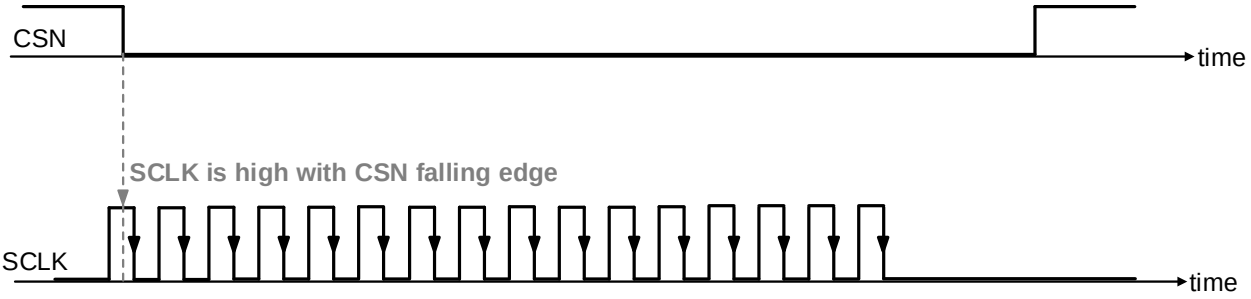
For a correct SPI communication:

- SCLK must be Low for a minimum t_{BEF} before CSN falling edge and t_{lead} after CSN falling edge
- SCLK must be Low for a minimum t_{lag} before CSN rising edge and t_{BEH} after CSN rising edge

Case 1: Correct SCLK signal



Case 2: Erroneous incoming clock signal



Case 3: Erroneous clock signal during CSN rising edge

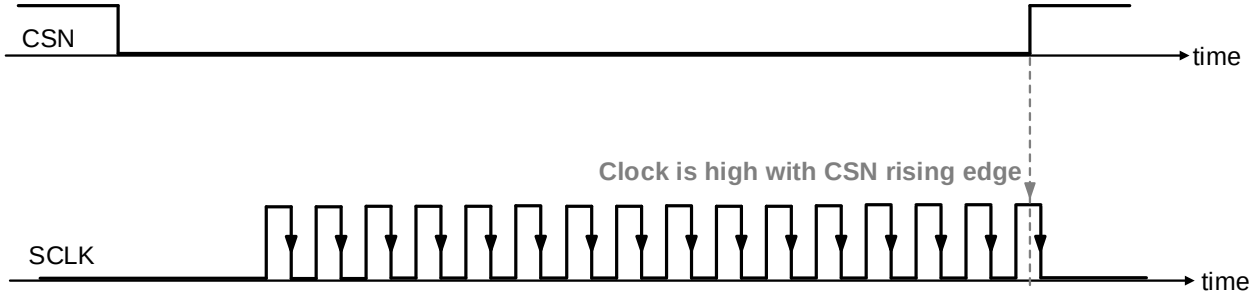


Figure 15. Clock Polarity Error

SPI with Independent Slave Configuration

In an independent slave configuration, the microcontroller controls the CSN of each slave individually (Figure 16).

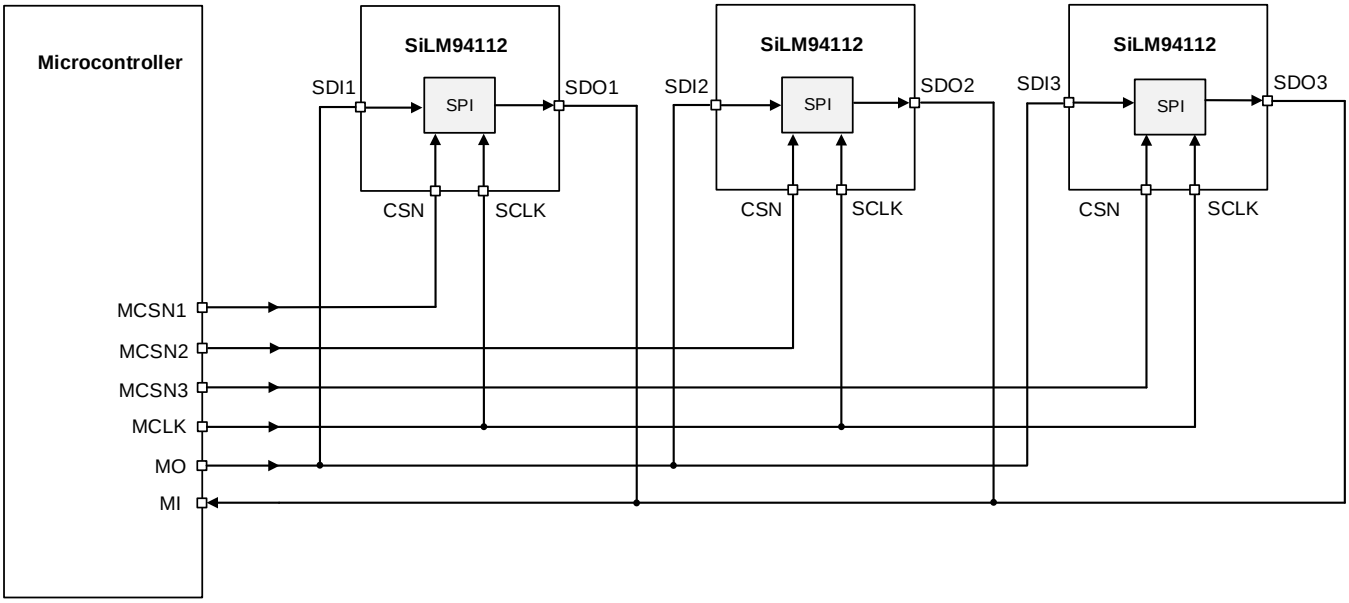


Figure 16. SPI with independent slave configuration

Each SPI communication starts with one address byte followed by one data byte (Figure 17).The LSB of the data byte must be set to '1'.The address bytes specifies:

- The type of operation: READ ONLY (OP bit =0) or READ/ WRITE (OP bit = 1) of the configuration bits, and READ ONLY (OP bit =0) or READ & CLEAR (OP bit = 1) of the status bits.
- The target register address (A[6:2])

The Last Address Byte Token bit (LABT, Bit1 of the address byte) must be set to 1, as no daisy chain configuration is used.

While the microcontroller sends the address byte on SDI, SDO shifts out GEF and the Global Status Register.

A further data byte (Bit15...8) is allocated to either configure the half-bridges or retrieve status information of the SiLM94112-AQ.

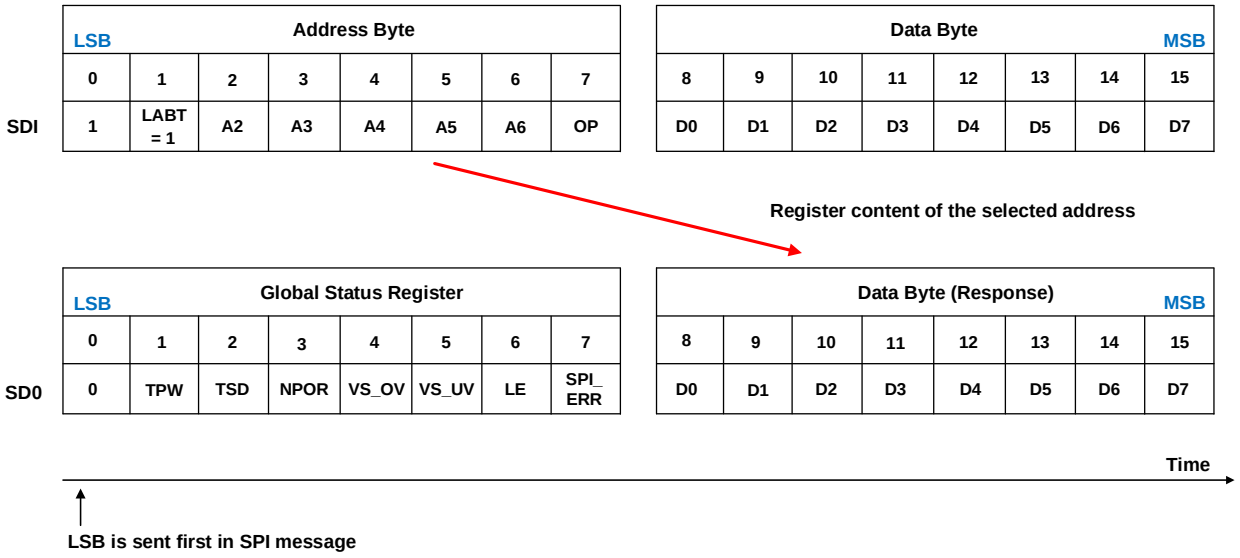


Figure 17. SPI Operation Mode with independent slave configuration

The in-frame response characteristic enables the microcontroller to read the contents of the addressed register within the SPI command. See Figure 17.

Daisy Chain Operation

The SiLM94112-AQ supports daisy chain operation with devices with the same SPI protocol. This section describes the daisy chain hardware configuration with three devices from the SiLM94112-AQ family (see Figure 18)

The master output (noted MO) is connected to a slave SDI and the first slave SDO is connected to the next slave SDI to form a chain. The SDO of the final slave in the chain will be connected to the master input (MI) to close the loop of the SPI communication frame. In daisy chain configuration, a single chip select, CSN, and clock signal, SCLK, connected in parallel to each slave device, are used by the microcontroller to control or access the SPI devices.

In this configuration, the Master Output must send the address bytes and data bytes in the following order:

- All address bytes must be sent first:

  – Address Byte 1 (for SiLM94112-AQ_1) is sent first, followed by Address Byte 2 (for SiLM94112-AQ_2) etc,...

  – The LABT bit of the last address byte must be 1, while the LABT bit of all the other address bytes must

be 0

- The data bytes are sent all together once all address bytes have been transmitted: Data Byte 1 (for

SiLM94112-AQ_1) is sent first, followed by Data Byte 2 (for SiLM94112-AQ_2) etc,...

Note: The signal on the SDI pin of the first IC in daisy chain (and in non-daisy chain mode), must be Low at the beginning of the SPI frame (between CSN falling edge and the first SCLK rising edge). This is because each Global Error Flag in daisy chain operation is implemented in OR logic.

The Master Input (MI), which is connected to the SDO of the last device in the daisy chain receives:

- A logic OR combination of all Global Error Flags (GEF), at the beginning of the SPI frame, between CSN falling edge and the first SCLK rising edge
- The logic OR combination of the GEFs is followed by the Global Status Registers in reverse order. In other words, MI receives first the Global Status Register of the last device of the daisy chain
- Once all Global Status Registers are received, MI receives the response bytes corresponding to the respective address and data bytes in reverse order. For example, if the daisy chain consists of three devices with SDO or SiLM94112-AQ_3 connected to MI, the master receives first the Response Byte 3 of SiLM94112-AQ_3 (corresponding to Address Byte 3 and Data Byte 3) followed by the Response Byte 2 of SiLM94112-AQ_2 and finally the Response Byte 1 of SiLM94112-AQ_1.

An example of an SPI frame with three devices from the SiLM941xy family is shown in Figure 19.

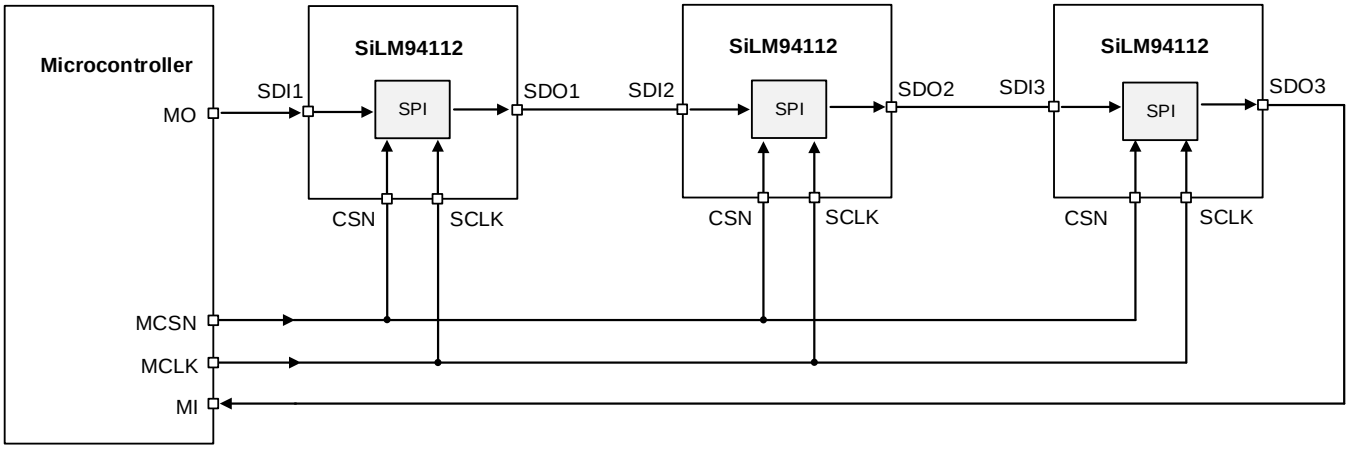


Figure 18. Example of daisy chain hardware configuration with devices from the SiLM941xy family

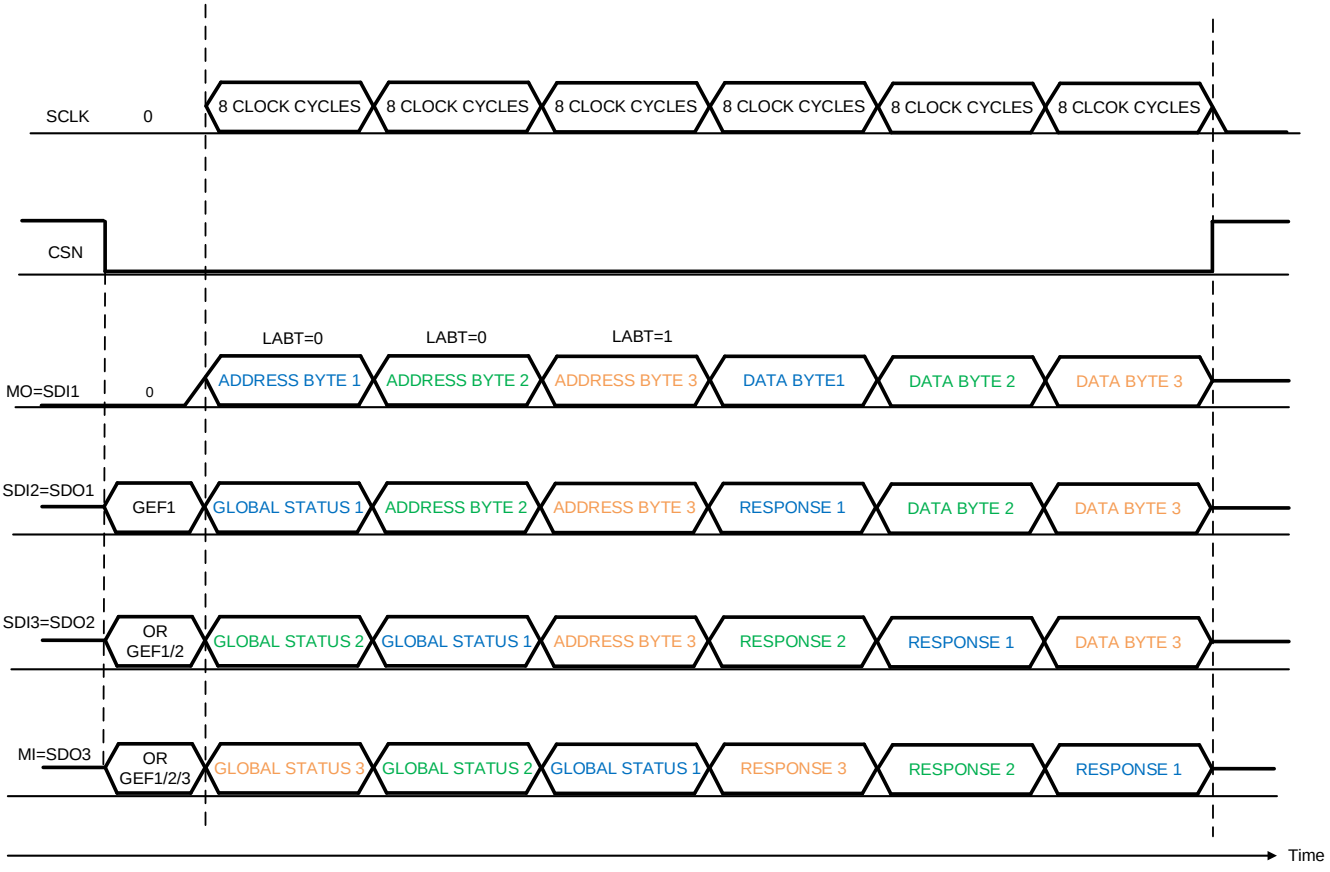


Figure 19. SPI frame with three devices of the SiLM941xy family

Like in the individual slave configuration, it is possible to check if one or several SiLM94112-AQ have detected a fault condition by reading the logic OR combination of all the Global Error Flags when CSN goes Low without any clock cycle (Figure 20).

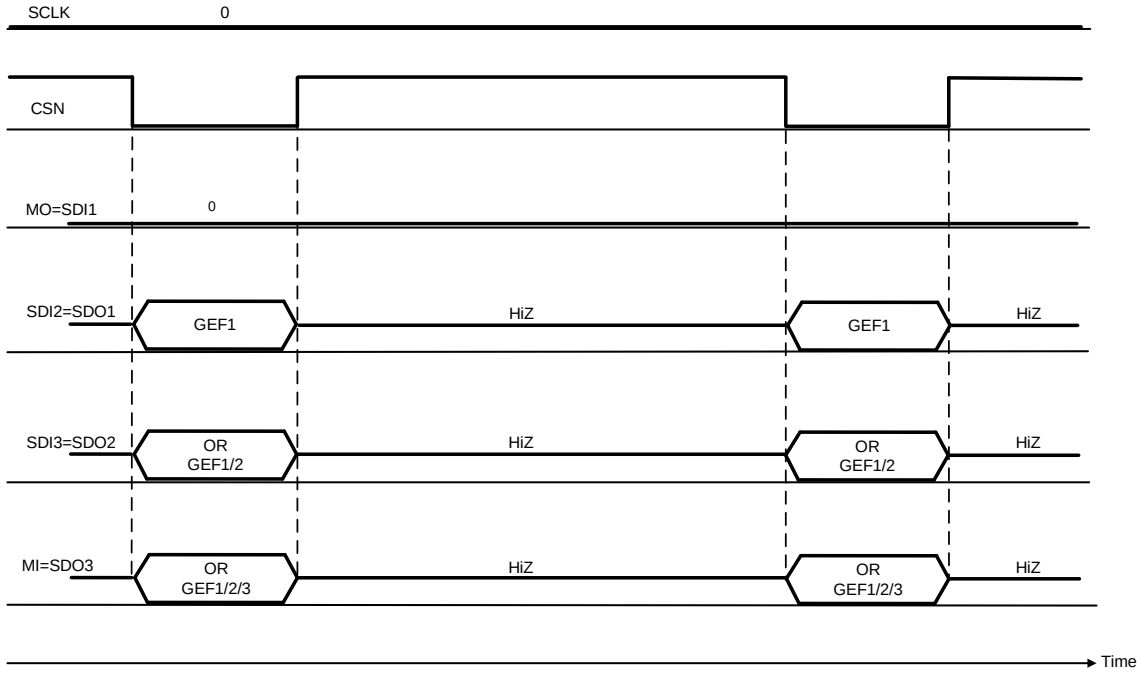


Figure 20. Global Error Flag with zero SCLK clock cycle in daisy chain consisting only of SiLM941xy devices

Note: Some SPI protocol errors such as the LSB of an address byte is wrongly equal to 0, may be reported in the SPI_ERR bit of another device in the daisy chain. In this case some devices might accept wrong data during the corrupted SPI frame. Therefore, if one of the devices in the daisy chain reports an SPI error, it is recommended to verify the content of the registers of all devices

Status Register Change During SPI Communication

If a new failure occurs after the transfer of the data byte(s), i.e. between the end of the last address byte and the CSN rising edge, this failure will be reported in the next SPI frame (see example in Figure 21).

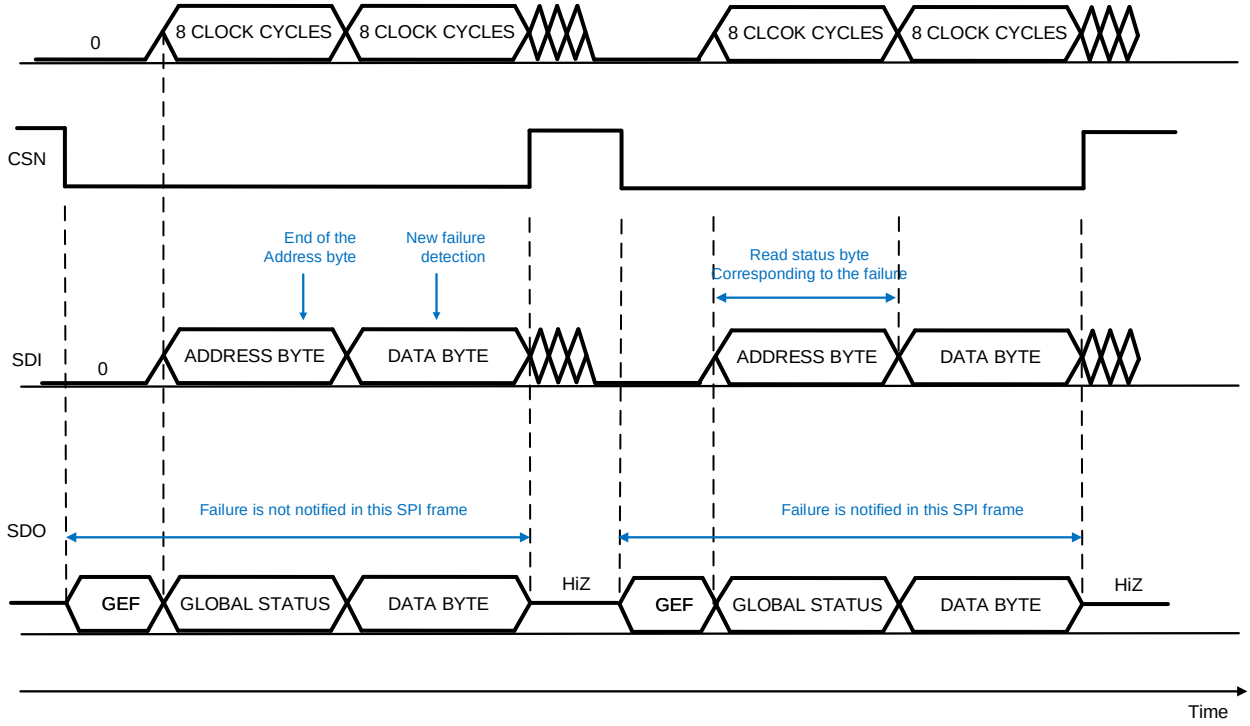


Figure 21. Status register change during transfer of data byte - Example in independent slave configuration

No information is lost, even if a status register is changed during a SPI frame, in particular during a Read and Clear command. For example:

- the microcontroller sends a Read and Clear command to a status register
- the SiLM94112-AQ detects during the transfer the data byte(s) a new fault condition, which is normally reported in the target status register

The incoming Clear command will be ignored, so that the microcontroller can read the new failure in the subsequent SPI frames.

Data inconsistency between the Global Status Register and the data byte (status register) within the same SPI frame is possible if:

- an open load or overcurrent error is detected during the transfer of the data byte
- the target status register corresponds to the new detected failure

In this case the new failure:

- is not reported in the Global Status Register of the current SPI frame but in the next one
- is reported in the data byte of the current SPI frame

An example in Figure 22 shows more details.

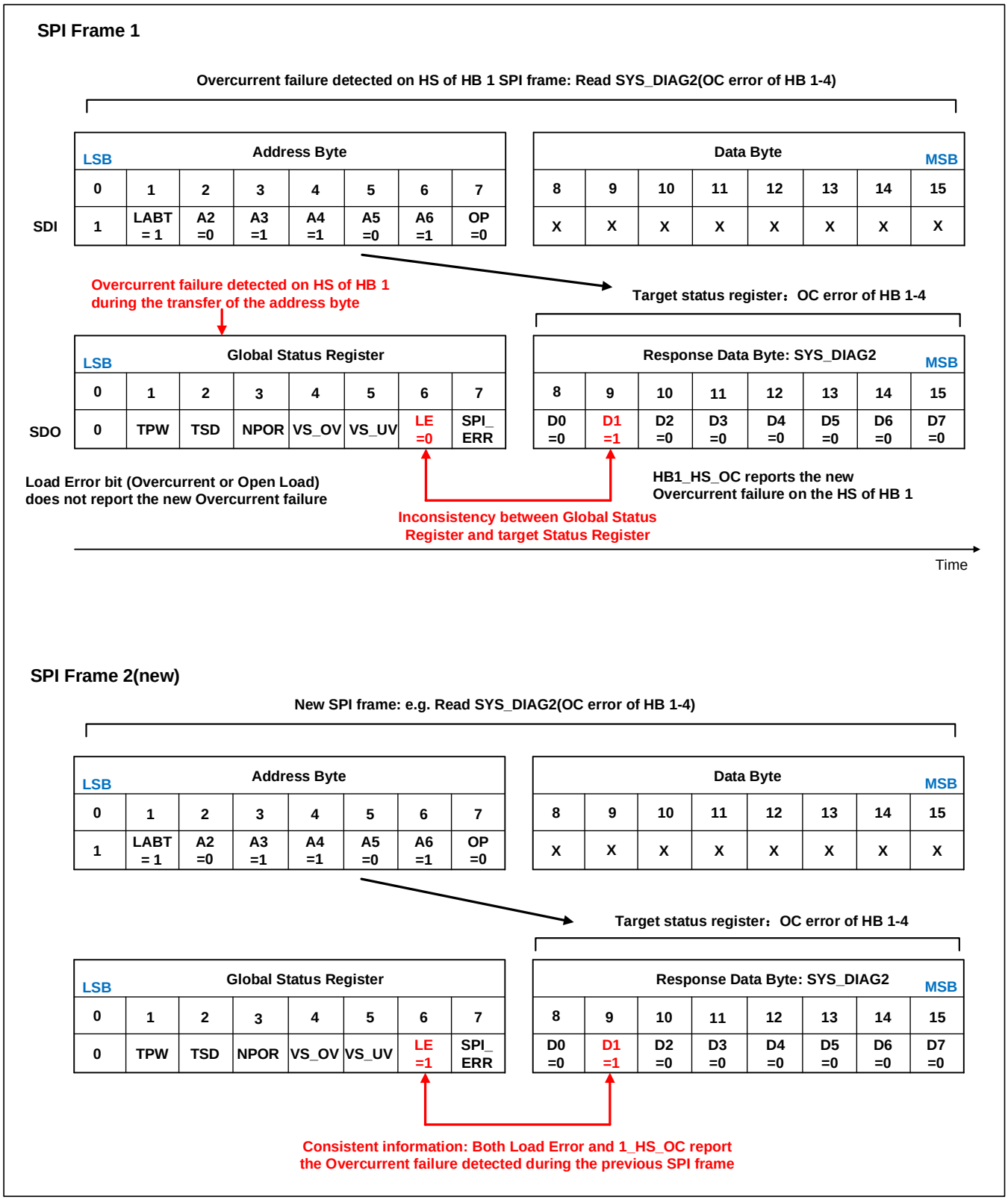


Figure 22. Example of inconsistency between Global Error Flag and Status Register when a status bit is changed during the transfer of an address byte

SPI Bit Mapping

The SPI Registers have been mapped as shown in Figure 23 and Figure 24 respectively. The control registers are READ/ WRITE registers. To set the control register to READ, bit 7 of the address byte (OP bit) must be programmed to '0', otherwise '1' for WRITE. The status registers are READ/CLEAR registers. To CLEAR any Status Register, bit 7 of the address byte must be set to '1', otherwise '0' for READ.

BIT	Data Bits 15-8	A7	A6	A5	A4	A3	A2	A1	A0
	Configuration & Status Information	Access type A7(OP)	A6-A0						
TYPE	8 Data Bits [D7…D0]	8 Address Bits [A7…A0]							
CONTROL REGISTERS	HB_ACT_1_CTRL	read/write	0	0	0	0	0	LABT	1
	HB_ACT_2_CTRL	read/write	1	0	0	0	0	LABT	1
	HB_ACT_3_CTRL	read/write	0	1	0	0	0	LABT	1
	HB_MODE_1_CTR	read/write	1	1	0	0	0	LABT	1
	HB_MODE_2_CTR	read/write	0	0	1	0	0	LABT	1
	HB_MODE_3_CTR	read/write	1	0	1	0	0	LABT	1
	PWM_CH_FREQ_CTR	read/write	0	1	1	0	0	LABT	1
	PWM1_DC_CTRL	read/write	1	1	1	0	0	LABT	1
	PWM2_DC_CTRL	read/write	0	0	0	1	0	LABT	1
	PWM3_DC_CTRL	read/write	1	0	0	1	0	LABT	1
	CONFIG_CTRL	read	1	1	0	0	1	LABT	1
	OVP2_2k_CTRL	read/write	0	0	0	1	1	LABT	1
	Reserved	read/write	1	0	0	1	1	LABT	1
	OLDN_DT_SR_CTRL	read/write	0	0	1	1	1	LABT	1
	Reserved	read/write	1	0	1	1	1	LABT	1
STATUS REGISTERS	SYS_DIAG_1 : Global status 1	read/clear	0	0	1	1	0	LABT	1
	SYS_DIAG_2: OP ERROR_1_STAT	read/clear	1	0	1	1	0	LABT	1
	SYS_DIAG_3: OP ERROR_2_STAT	read/clear	0	1	1	1	0	LABT	1
	SYS_DIAG_4: OP ERROR_3_STAT	read/clear	1	1	1	1	0	LABT	1
	SYS_DIAG_5: OP ERROR_4_STAT	read/clear	0	0	0	0	1	LABT	1
	SYS_DIAG_6:OP ERROR_5_STAT	read/clear	1	0	0	0	1	LABT	1
	SYS_DIAG_7: OP ERROR_6_STAT	read/clear	0	1	0	0	1	LABT	1

Figure 23. SiLM94112-AQ SPI Register mapping

BIT	15	14	13	12	11	10	9	8
	D7	D6	D5	D4	D3	D2	D1	D0
CONTROL REGISTERS								
HB_ACT_1_CTRL	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
HB_ACT_2_CTRL	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
HB_ACT_3_CTRL	HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN
HB_MODE_1_CTR	HB4_MODE_1	HB4_MODE_0	HB3_MODE_1	HB3_MODE_0	HB2_MODE_1	HB2_MODE_0	HB1_MODE_1	HB1_MODE_0
HB_MODE_2_CTR	HB8_MODE_1	HB8_MODE_0	HB7_MODE_1	HB7_MODE_0	HB6_MODE_1	HB6_MODE_0	HB5_MODE_1	HB5_MODE_0
HB_MODE_3_CTR	HB12_MODE_1	HB12_MODE_0	HB11_MODE_1	HB11_MODE_0	HB10_MODE_1	HB10_MODE_0	HB9_MODE_1	HB9_MODE_0
PWM_CH_FREQ_CTR	FM_CLK_MOD1	FM_CLK_MOD0	PWM_CH3_FREQ_1	PWM_CH3_FREQ_0	PWM_CH2_FREQ_1	PWM_CH2_FREQ_0	PWM_CH1_FREQ_1	PWM_CH1_FREQ_0
PWM1_DC_CTRL	PWM1_DC_CTRL<7:0>							
PWM2_DC_CTRL	PWM2_DC_CTRL<7:0>							
PWM3_DC_CTRL	PWM3_DC_CTRL<7:0>							
CONFIG_CTRL	Reserved	Reserved	Reserved	Reserved	DEV_ID3	DEV_ID2	DEV_ID1	DEV_ID0
OVP2_2k_CTRL	EXT_OVP	PWM_CH3_2k	PWM_CH2_2k	PWM_CH1_2k	Reserved	Reserved	Reserved	Reserved
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
OLDN_DT_SR_CTRL	Reserved	Reserved	DIS_OL_NEG	DTIME_SEL	Reserved	SR_2	SR_1	SR_0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
STATUS REGISTERS								
SYS_DIAG_1：Global status 1	SPI_ERR	LE	VS_UV	VS_OV	NPOR	TSD	TPW	Reserved
SYS_DIAG_2:OP ERROR_1_STAT	HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
SYS_DIAG_3: OP	HB8_HS_OC	HB8_LS_OC	HB7_HS_OC	HB7_LS_OC	HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC

BIT	15	14	13	12	11	10	9	8
ERROR_2 _STAT								
SYS_DIAG _4: OP ERROR_3 _STAT	HB12_ HS_OC	HB12_L S_OC	HB11_HS _OC	HB11_LS _OC	HB10_HS _OC	HB10_LS _OC	HB9_HS_ OC	HB9_LS_ OC
SYS_DIAG _5: OP ERROR_4 _STAT	HB4_H S_OL	HB4_L S_OL	HB3_HS_ OL	HB3_LS_ OL	HB2_HS_ OL	HB2_LS_ OL	HB1_HS_ OL	HB1_LS_ OL
SYS_DIAG _6:OP ERROR_5 _STAT	HB8_H S_OL	HB8_L S_OL	HB7_HS_ OL	HB7_LS_ OL	HB6_HS_ OL	HB6_LS_ OL	HB5_HS_ OL	HB5_LS_ OL
SYS_DIAG _7: OP ERROR_6 _STAT	HB12_ HS_OL	HB12_L S_OL	HB11_HS _OL	HB11_LS _OL	HB10_HS _OL	HB10_LS _OL	HB9_HS_ OL	HB9_LS_ OL

Figure 24. SiLM94112-AQ Bit Mapping

SPI Control Registers

The Control Registers have a READ/WRITE access:

- The 'POR' value is defined by the register content after a POR or device Reset
  – The default value of all control registers is 0000 0000_B
- One 16-bit SPI command consists of two bytes (see Figure 23 and Figure 24), i.e.
  – an address byte
  – followed by a data byte
- The control bits are not cleared or changed automatically by the device. This must be done by the microcontroller via SPI programming.
- Reading a register is done byte wise by setting the SPI bit 7 to "0" (= READ ONLY).
- Writing to a register is done byte wise by setting the SPI bit 7 to "1"

Table 6. Half-bridge output control 1 Register

HB_ACT_1_CTRL ([OP] 000 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB4_HS_EN	r/w	Half-bridge output 4 high side switch enable 0 HS4 OFF/ High-Z (default value) 1 HS4 ON
[6]	HB4_LS_EN	r/w	Half-bridge output 4 low side switch enable 0 LS4 OFF/ High-Z (default value) 1 LS4 ON
[5]	HB3_HS_EN	r/w	Half-bridge output 3 high side switch enable 0 HS3 OFF/ High-Z (default value) 1 HS3 ON
[4]	HB3_LS_EN	r/w	Half-bridge output 3 low side switch enable 0 LS3 OFF/ High-Z (default value) 1 LS3 ON
[3]	HB2_HS_EN	r/w	Half-bridge output 2 high side switch enable 0 HS2 OFF/ High-Z (default value) 1 HS2 ON
[2]	HB2_LS_EN	r/w	Half-bridge output 2 low side switch enable 0 LS2 OFF/ High-Z (default value) 1 LS2 ON
[1]	HB1_HS_EN	r/w	Half-bridge output 1 high side switch enable 0 HS1 OFF/ High-Z (default value) 1 HS1 ON
[0]	HB1_LS_EN	r/w	Half-bridge output 1 low side switch enable 0 LS1 OFF/ High-Z (default value) 1 LS1 ON

Note: The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS_EN and HS_EN bits of a given half-bridge are set, the logic turns off this half-bridge.

Table 7. Half-bridge output control 2 Register

HB_ACT_2_CTRL([OP] 100 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB8_HS_EN	r/w	Half-bridge output 8 high side switch enable 0 HS8 OFF/ High-Z (default value) 1 HS8 ON
[6]	HB8_LS_EN	r/w	Half-bridge output 8 low side switch enable 0 LS8 OFF/ High-Z (default value) 1 LS8 ON
[5]	HB7_HS_EN	r/w	Half-bridge output 7 high side switch enable 0 HS7 OFF/ High-Z (default value) 1 HS7 ON
[4]	HB7_LS_EN	r/w	Half-bridge output 7 low side switch enable 0 LS7 OFF/ High-Z (default value) 1 LS7 ON
[3]	HB6_HS_EN	r/w	Half-bridge output 6 high side switch enable 0 HS6 OFF/ High-Z (default value) 1 HS6 ON
[2]	HB6_LS_EN	r/w	Half-bridge output 6 low side switch enable 0 LS6 OFF/ High-Z (default value) 1 LS6 ON
[1]	HB5_HS_EN	r/w	Half-bridge output 5 high side switch enable 0 HS5 OFF/ High-Z (default value) 1 HS5 ON
[0]	HB5_LS_EN	r/w	Half-bridge output 5 low side switch enable 0 LS5 OFF/ High-Z (default value) 1 LS5 ON

Note: The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS_EN and HS_EN bits of a given half-bridge are set, the logic turns off this half-bridge.

Table 8. Half-bridge output control 3 Register

HB_ACT_3_CTRL([OP] 010 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB12_HS_EN	r/w	Half-bridge output 12 high side switch enable 0 HS12 OFF/ High-Z (default value) 1 HS12 ON
[6]	HB12_LS_EN	r/w	Half-bridge output 12 low side switch enable 0 LS12 OFF/ High-Z (default value) 1 LS12 ON
[5]	HB11_HS_EN	r/w	Half-bridge output 11 high side switch enable 0 HS11 OFF/ High-Z (default value) 1 HS11 ON
[4]	HB11_LS_EN	r/w	Half-bridge output 11 low side switch enable 0 LS11 OFF/ High-Z (default value) 1 LS11 ON
[3]	HB10_HS_EN	r/w	Half-bridge output 10 high side switch enable 0 HS10 OFF/ High-Z (default value) 1 HS10 ON
[2]	HB10_LS_EN	r/w	Half-bridge output 10 low side switch enable 0 LS10 OFF/ High-Z (default value) 1 LS10 ON
[1]	HB9_HS_EN	r/w	Half-bridge output 9 high side switch enable 0 HS9 OFF/ High-Z (default value) 1 HS9 ON
[0]	HB9_LS_EN	r/w	Half-bridge output 9 low side switch enable 0 LS9 OFF/ High-Z (default value) 1 LS9 ON

Note: The simultaneous activation of both HS and LS switch within a half-bridge is prevented by the digital block to avoid cross current. If both LS_EN and HS_EN bits of a given half-bridge are set, the logic turns off this half-bridge.

Table 9. Half-bridge output mode control 1 Register

HB_MODE_1_CTRL ([OP] 110 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-6]	HB4_MODEn (n = 1,0)	r/w	Half-bridge output 4 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[5-4]	HB3_MODEn (n = 1,0)	r/w	Half-bridge output 3 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[3-2]	HB2_MODEn (n = 1,0)	r/w	Half-bridge output 2 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[1-0]	HB1_MODEn (n = 1,0)	r/w	Half-bridge output 1 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3

Table 10. Half-bridge output mode control 2 Register

HB_MODE_2_CTRL ([OP] 001 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-6]	HB8_MODEn (n = 1,0)	r/w	Half-bridge output 8 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[5-4]	HB7_MODEn (n = 1,0)	r/w	Half-bridge output 7 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[3-2]	HB6_MODEn (n = 1,0)	r/w	Half-bridge output 6 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[1-0]	HB5_MODEn (n = 1,0)	r/w	Half-bridge output 5 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3

Table 11. Half-bridge output mode control 3 Register

HB_MODE_3_CTRL ([OP] 101 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-6]	HB12_MODEn (n = 1,0)	r/w	Half-bridge output 12 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[5-4]	HB11_MODEn (n = 1,0)	r/w	Half-bridge output 11 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[3-2]	HB10_MODEn (n = 1,0)	r/w	Half-bridge output 10 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3
[1-0]	HB9_MODEn (n = 1,0)	r/w	Half-bridge output 9 mode select 00 No PWM (default value) 01 PWM control with PWM Channel 1 10 PWM control with PWM Channel 2 11 PWM control with PWM Channel 3

Table 12. PWM channel frequency select Register

PWM_CH_FREQ_CTRL ([OP] 011 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-6]	FM_CLK_MODn (n = 1,0)	r/w	FM Modulation Enable[1] 00 No modulation (default) 01 Modulation frequency 15.625kHz 10 Modulation frequency 31.25kHz 11 Modulation frequency 62.5kHz
[5-4]	PWM_CH3_FREQ_n (n = 1,0)	r/w	PWM Channel 3 frequency select 00 PWM is stopped and off (default value) 01 PWM frequency 1 : 80Hz 10 PWM frequency 2 : 100Hz 11 PWM frequency 3 : 200Hz
[3-2]	PWM_CH2_FREQ_n (n = 1,0)	r/w	PWM Channel 2 frequency select 00 PWM is stopped and off (default value) 01 PWM frequency 1 : 80Hz 10 PWM frequency 2 : 100Hz 11 PWM frequency 3 : 200Hz
[1-0]	PWM_CH1_FREQ_n (n = 1,0)	r/w	PWM Channel 1 frequency select 00 PWM is stopped and off (default value) 01 PWM frequency 1 : 80Hz 10 PWM frequency 2 : 100Hz 11 PWM frequency 3 : 200Hz

1 Not subject to production test, guaranteed by design. Frequency may deviate by ±10%

Table 13. PWM channel 1 duty cycle configuration Register

PWM1_DC_CTRL ([OP] 111 00[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-0]	PWM1_DC_CTRLn	r/w	PWM Channel 1 Duty Cycle configuration (bit7=MSB; bit0) 0000 0000 100% OFF (default value) xxxx xxxx parts of 255 ON 1111 1111 100% ON

Table 14. PWM channel 2 duty cycle configuration Register

PWM2_DC_CTRL ([OP] 000 10[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-0]	PWM2_DC_CTRLn	r/w	PWM Channel 2 Duty Cycle configuration (bit7=MSB; bit0) 0000 0000 100% OFF (default value) xxxx xxxx parts of 255 ON 1111 1111 100% ON

Table 15. PWM channel 3 duty cycle configuration Register

PWM3_DC_CTRL ([OP] 100 10[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-0]	PWM3_DC_CTRLn	r/w	PWM Channel 3 Duty Cycle configuration (bit7=MSB; bit0) 0000 0000 100% OFF (default value) xxxx xxxx parts of 255 ON 1111 1111 100% ON

Table 16. Device Configuration Control Register

CONFIG_CTRL ([OP] 110 01[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-4]	Reserved	r	Always reads as ‘0’.
[3-0]	DEV_IDn	r/w	Device/ derivative identifier Note: These bits can be used to verify the silicon content of the device 1000 SiLM94112 chip 1001 SiLM94110 chip 1010 SiLM94108 chip 1011 SiLM94106 chip 1100 SiLM94104 chip 1101 SiLM94103 chip 1110 reserved 1111 reserved

Table 17. OVP2 and 2kHz Control Register

OVP2_2k_CTRL ([OP] 000 11[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	EXT_OVP	r/w	Overvoltage protection configuration 0 = Overvoltage protection threshold is at 21 V (default value) 1 = Overvoltage protection threshold is at 33 V
[6]	PWM_CH3_2k	r/w	PWM Channel 3 frequency select 0 = PWM Channel 3 frequency is decided by Register PWM_CH_FREQ_CTRL (default value) 1 = PWM frequency is 2000 Hz
[5]	PWM_CH2_2k	r/w	PWM Channel 2 frequency select 0 = PWM Channel 2 frequency is decided by Register PWM_CH_FREQ_CTRL (default value) 1 = PWM frequency is 2000 Hz
[4]	PWM_CH1_2k	r/w	PWM Channel 1 frequency select 0 = PWM Channel 1 frequency is decided by Register PWM_CH_FREQ_CTRL (default value) 1 = PWM frequency is 2000 Hz
[3]	Reserved	R	Always reads as ‘0’.
[2]	Reserved	R	Always reads as ‘0’.
[1]	Reserved	R	Always reads as ‘0’.
[0]	Reserved	R	Always reads as ‘0’.

Table 18. OLDN,DT and SR Control Register

OLDN_DT_SR_CTRL ([OP] 001 11[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7-6]	Reserved	r	Always reads as '0'.
[5]	DIS_OL_NEG	r/w	0 = Active Free Wheeling OLD mode is enabled (default value) 1 = Active Free Wheeling OLD mode is disabled
[4]	DTIME_SET	r/w	Dead Time DHL/DLH Setting 0 = 128us (default value) 1 = 32us
[3]	Reserved	r	Always reads as '0'.
[2-0]	SR_CTRL	r/w	Slew Rate Control 000 =0.35V/us (default value) 001 =0.2V/us 010 =0.5V/us 011 =0.6V/us 100 =1.7V/us 101 =1V/us 110 =2.4V/us 111 =3V/us

SPI Status Registers

The Status Registers have a READ/CLEAR access:

• The 'POR Value' of the Status registers (content after a POR or device Reset) and is 0000 0000B.

• One 16-bit SPI command consists of two bytes (see Figure 25 and Figure 26), i.e.

– an address byte

– followed by a data byte

• Reading a register is done byte wise by setting the SPI bit 7 of the address byte to "0" (= Read Only).

• Clearing a register is done byte wise by setting the SPI bit 7 of the address byte to "1".

• SPI status registers are not cleared automatically by the device. This must be done by the microcontroller via SPI command.

Table 19. Global status 1 Register

SYS_DIAG1 ([OP] 001 10[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	SPI_ERR	r/c	SPI error detection 0 No SPI protocol error is detected (default value). 1 An SPI protocol error is detected.
[6]	LE	r	Load error detection (logic OR combination of Open Load and Overcurrent) 0 No Open Load and no Overcurrent detected (default value) 1 Open Load or Overcurrent detected in at least one of the power outputs. Error latched. Faulty output is latched off in case of Overcurrent
[5]	VS_UV	r/c	VS Undervoltage error detection 0 No undervoltage on VS detected (default value) 1 Undervoltage on VS detected. Error latched and all outputs disabled.
[4]	VS_OV	r/c	VS Overvoltage error detection 0 No overvoltage on VS detected (default value) 1 Overvoltage on VS detected. Error latched and all outputs disabled.
[3]	NPOR	r/c	Not Power On Reset (NPOR) detection 0 POR on EN or VDD supply rail (default value) 1 No POR
[2]	TSD	r/c	Temperature shutdown error detection 0 Junction temperature below temperature shutdown threshold (default value) 1 Junction temperature has reached temperature shutdown threshold. Error latched and all outputs disabled.
[1]	TPW	r/c	Temperature pre-warning error detection 0 Junction temperature below temperature pre-warning threshold (default value) 1 Junction temperature has reached temperature pre-warning threshold.
[0]	Reserved	r	Bit reserved. Always reads ‘0’.

Note: The LE bit in the Global Status register is read only. It reflects an OR combination of the respective open load and overcurrent errors of the half-bridge channels. If all OC/ OL bits of the respective high-side and low-side channels are cleared to ‘0’, the LE bit will be automatically update.

Table 20. Overcurrent error status of half-bridge outputs 1 – 4 Register

SYS_DIAG2 OP_ERROR_1_STAT ([OP] 101 10[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB4_HS_OC	r/c	High-side (HS) switch of half-bridge 4 overcurrent detection 0 No error on HS4 switch (default value) 1 Overcurrent detected on HS4 switch. Error latched and HS4 disabled
[6]	HB4_LS_OC	r/c	Low-side (LS) switch of half-bridge 4 overcurrent detection 0 No error on LS4 switch (default value) 1 Overcurrent detected on LS4 switch. Error latched and LS4 disabled
[5]	HB3_HS_OC	r/c	High-side (HS) switch of half-bridge 3 overcurrent detection 0 No error on HS3 switch (default value) 1 Overcurrent detected on HS3 switch. Error latched and HS3 disabled
[4]	HB3_LS_OC	r/c	Low-side (LS) switch of half-bridge 3 overcurrent detection 0 No error on LS3 switch (default value) 1 Overcurrent detected on LS3 switch. Error latched and LS3 disabled
[3]	HB2_HS_OC	r/c	High-side (HS) switch of half-bridge 2 overcurrent detection 0 No error on HS2 switch (default value) 1 Overcurrent detected on HS2 switch. Error latched and HS2 disabled
[2]	HB2_LS_OC	r/c	Low-side (LS) switch of half-bridge 2 overcurrent detection 0 No error on LS2 switch (default value) 1 Overcurrent detected on LS2 switch. Error latched and LS2 disabled
[1]	HB1_HS_OC	r/c	High-side (HS) switch of half-bridge 1 overcurrent detection 0 No error on HS1 switch (default value) 1 Overcurrent detected on HS1 switch. Error latched and HS1 disabled
[0]	HB1_LS_OC	r/c	Low-side (LS) switch of half-bridge 1 overcurrent detection 0 No error on LS1 switch (default value) 1 Overcurrent detected on LS1 switch. Error latched and LS1 disabled

Table 21. Overcurrent error status of half-bridge outputs 5 – 8 Register

SYS_DIAG3 OP_ERROR_2_STAT ([OP] 011 10[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB8_HS_OC	r/c	High-side (HS) switch of half-bridge 8 overcurrent detection 0 No error on HS8 switch (default value) 1 Overcurrent detected on HS8 switch. Error latched and HS8 disabled
[6]	HB8_LS_OC	r/c	Low-side (LS) switch of half-bridge 8 overcurrent detection 0 No error on LS8 switch (default value) 1 Overcurrent detected on LS8 switch. Error latched and LS8 disabled
[5]	HB7_HS_OC	r/c	High-side (HS) switch of half-bridge 7 overcurrent detection 0 No error on HS7 switch (default value) 1 Overcurrent detected on HS7 switch. Error latched and HS7 disabled
[4]	HB7_LS_OC	r/c	Low-side (LS) switch of half-bridge 7 overcurrent detection 0 No error on LS7 switch (default value) 1 Overcurrent detected on LS7 switch. Error latched and LS7 disabled
[3]	HB6_HS_OC	r/c	High-side (HS) switch of half-bridge 6 overcurrent detection 0 No error on HS6 switch (default value) 1 Overcurrent detected on HS6 switch. Error latched and HS6 disabled
[2]	HB6_LS_OC	r/c	Low-side (LS) switch of half-bridge 6 overcurrent detection 0 No error on LS6 switch (default value) 1 Overcurrent detected on LS6 switch. Error latched and LS6 disabled
[1]	HB5_HS_OC	r/c	High-side (HS) switch of half-bridge 5 overcurrent detection 0 No error on HS5 switch (default value) 1 Overcurrent detected on HS5 switch. Error latched and HS5 disabled
[0]	HB5_LS_OC	r/c	Low-side (LS) switch of half-bridge 5 overcurrent detection 0 No error on LS5 switch (default value) 1 Overcurrent detected on LS5 switch. Error latched and LS5 disabled

Table 22. Overcurrent error status of half-bridge outputs 9 – 12 Register

SYS_DIAG4 OP_ERROR_3_STAT ([OP] 111 10[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB12_HS_OC	r/c	High-side (HS) switch of half-bridge 12 overcurrent detection 0 No error on HS12 switch (default value) 1 Overcurrent detected on HS12 switch. Error latched and HS12 disabled
[6]	HB12_LS_OC	r/c	Low-side (LS) switch of half-bridge 12 overcurrent detection 0 No error on LS12 switch (default value) 1 Overcurrent detected on LS12 switch. Error latched and LS12 disabled
[5]	HB11_HS_OC	r/c	High-side (HS) switch of half-bridge 11 overcurrent detection 0 No error on HS11 switch (default value) 1 Overcurrent detected on HS11 switch. Error latched and HS11 disabled
[4]	HB11_LS_OC	r/c	Low-side (LS) switch of half-bridge 11 overcurrent detection 0 No error on LS11 switch (default value) 1 Overcurrent detected on LS11 switch. Error latched and LS11 disabled
[3]	HB10_HS_OC	r/c	High-side (HS) switch of half-bridge 10 overcurrent detection 0 No error on HS10 switch (default value) 1 Overcurrent detected on HS10 switch. Error latched and HS10 disabled
[2]	HB10_LS_OC	r/c	Low-side (LS) switch of half-bridge 10 overcurrent detection 0 No error on LS10 switch (default value) 1 Overcurrent detected on LS10 switch. Error latched and LS10 disabled
[1]	HB9_HS_OC	r/c	High-side (HS) switch of half-bridge 9 overcurrent detection 0 No error on HS9 switch (default value) 1 Overcurrent detected on HS9 switch. Error latched and HS9 disabled
[0]	HB9_LS_OC	r/c	Low-side (LS) switch of half-bridge 9 overcurrent detection 0 No error on LS9 switch (default value) 1 Overcurrent detected on LS9 switch. Error latched and LS9 disabled

Table 23. Open load error status of half-bridge outputs 1 – 4 Register

SYS_DIAG5 OP_ERROR_4_STAT ([OP] 000 01[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB4_HS_OL	r/c	High-side (HS) switch of half-bridge 4 open load detection 0 No error on HS4 switch (default value) 1 Open load detected on HS4 switch. Error latched.
[6]	HB4_LS_OL	r/c	Low-side (LS) switch of half-bridge 4 open load detection 0 No error on LS4 switch (default value) 1 Open load detected on LS4 switch. Error latched.
[5]	HB3_HS_OL	r/c	High-side (HS) switch of half-bridge 3 open load detection 0 No error on HS3 switch (default value) 1 Open load detected on HS3 switch. Error latched.
[4]	HB3_LS_OL	r/c	Low-side (LS) switch of half-bridge 3 open load detection 0 No error on LS3 switch (default value) 1 Open load detected on LS3 switch. Error latched.
[3]	HB2_HS_OL	r/c	High-side (HS) switch of half-bridge 2 open load detection 0 No error on HS2 switch (default value) 1 Open load detected on HS2 switch. Error latched.
[2]	HB2_LS_OL	r/c	Low-side (LS) switch of half-bridge 2 open load detection 0 No error on LS2 switch (default value) 1 Open load detected on LS2 switch. Error latched.
[1]	HB1_HS_OL	r/c	High-side (HS) switch of half-bridge 1 open load detection 0 No error on HS1 switch (default value) 1 Open load detected on HS1 switch. Error latched.
[0]	HB1_LS_OL	r/c	Low-side (LS) switch of half-bridge 1 open load detection 0 No error on LS1 switch (default value) 1 Open load detected on LS1 switch. Error latched.

Table 24. Open load error status of half-bridge outputs 5 – 8 Register

SYS_DIAG6 OP_ERROR_5_STAT ([OP] 100 01[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB8_HS_OL	r/c	High-side (HS) switch of half-bridge 8 open load detection 0 No error on HS8 switch (default value) 1 Open load detected on HS8 switch. Error latched.
[6]	HB8_LS_OL	r/c	Low-side (LS) switch of half-bridge 8 open load detection 0 No error on LS8 switch (default value) 1 Open load detected on LS8 switch. Error latched.
[5]	HB7_HS_OL	r/c	High-side (HS) switch of half-bridge 7 open load detection 0 No error on HS7 switch (default value) 1 Open load detected on HS7 switch. Error latched.
[4]	HB7_LS_OL	r/c	Low-side (LS) switch of half-bridge 7 open load detection 0 No error on LS7 switch (default value) 1 Open load detected on LS7 switch. Error latched.
[3]	HB6_HS_OL	r/c	High-side (HS) switch of half-bridge 6 open load detection 0 No error on HS6 switch (default value) 1 Open load detected on HS6 switch. Error latched.
[2]	HB6_LS_OL	r/c	Low-side (LS) switch of half-bridge 6 open load detection 0 No error on LS6 switch (default value) 1 Open load detected on LS6 switch. Error latched.
[1]	HB5_HS_OL	r/c	High-side (HS) switch of half-bridge 5 open load detection 0 No error on HS5 switch (default value) 1 Open load detected on HS5 switch. Error latched.
[0]	HB5_LS_OL	r/c	Low-side (LS) switch of half-bridge 5 open load detection 0 No error on LS5 switch (default value) 1 Open load detected on LS5 switch. Error latched.

Table 25. Open load error status of half-bridge outputs 9 – 12 Register

SYS_DIAG7 OP_ERROR_6_STAT ([OP] 010 01[LABT]1)			
Bit	**Symbol**	**TYPE**	**Description**
[7]	HB12_HS_OL	r/c	High-side (HS) switch of half-bridge 12 open load detection 0 No error on HS12 switch (default value) 1 Open load detected on HS12 switch. Error latched.
[6]	HB12_LS_OL	r/c	Low-side (LS) switch of half-bridge 12 open load detection 0 No error on LS12 switch (default value) 1 Open load detected on LS12 switch. Error latched.
[5]	HB11_HS_OL	r/c	High-side (HS) switch of half-bridge 11 open load detection 0 No error on HS11 switch (default value) 1 Open load detected on HS11 switch. Error latched.
[4]	HB11_LS_OL	r/c	Low-side (LS) switch of half-bridge 11 open load detection 0 No error on LS11 switch (default value) 1 Open load detected on LS11 switch. Error latched.
[3]	HB10_HS_OL	r/c	High-side (HS) switch of half-bridge 10 open load detection 0 No error on HS10 switch (default value) 1 Open load detected on HS10 switch. Error latched.
[2]	HB10_LS_OL	r/c	Low-side (LS) switch of half-bridge 10 open load detection 0 No error on LS10 switch (default value) 1 Open load detected on LS10 switch. Error latched.
[1]	HB9_HS_OL	r/c	High-side (HS) switch of half-bridge 9 open load detection 0 No error on HS9 switch (default value) 1 Open load detected on HS9 switch. Error latched.
[0]	HB9_LS_OL	r/c	Low-side (LS) switch of half-bridge 9 open load detection 0 No error on LS9 switch (default value) 1 Open load detected on LS9 switch. Error latched.

APPLICATION INFORMATION

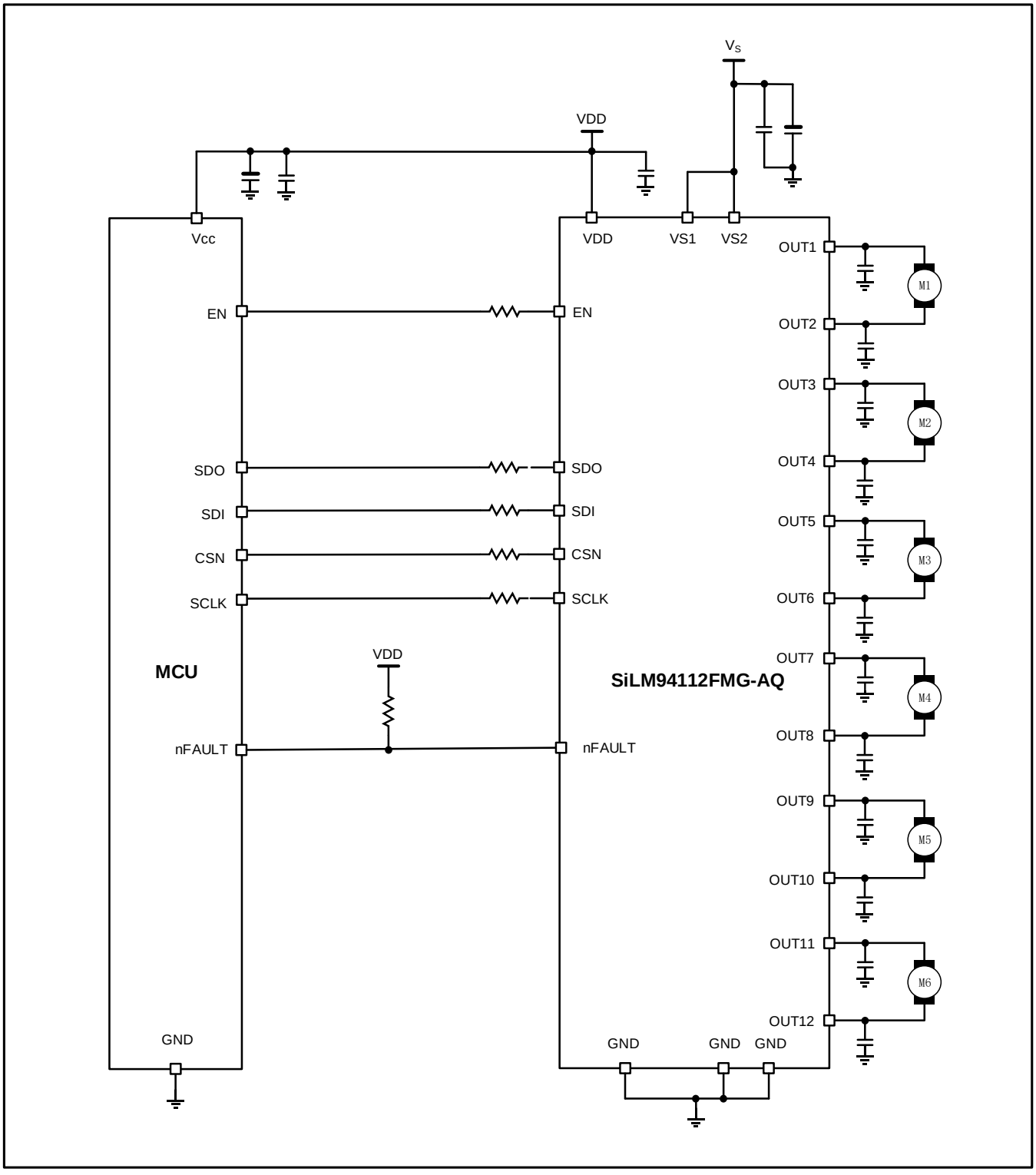


Figure 25. Application example for DC-motor loads

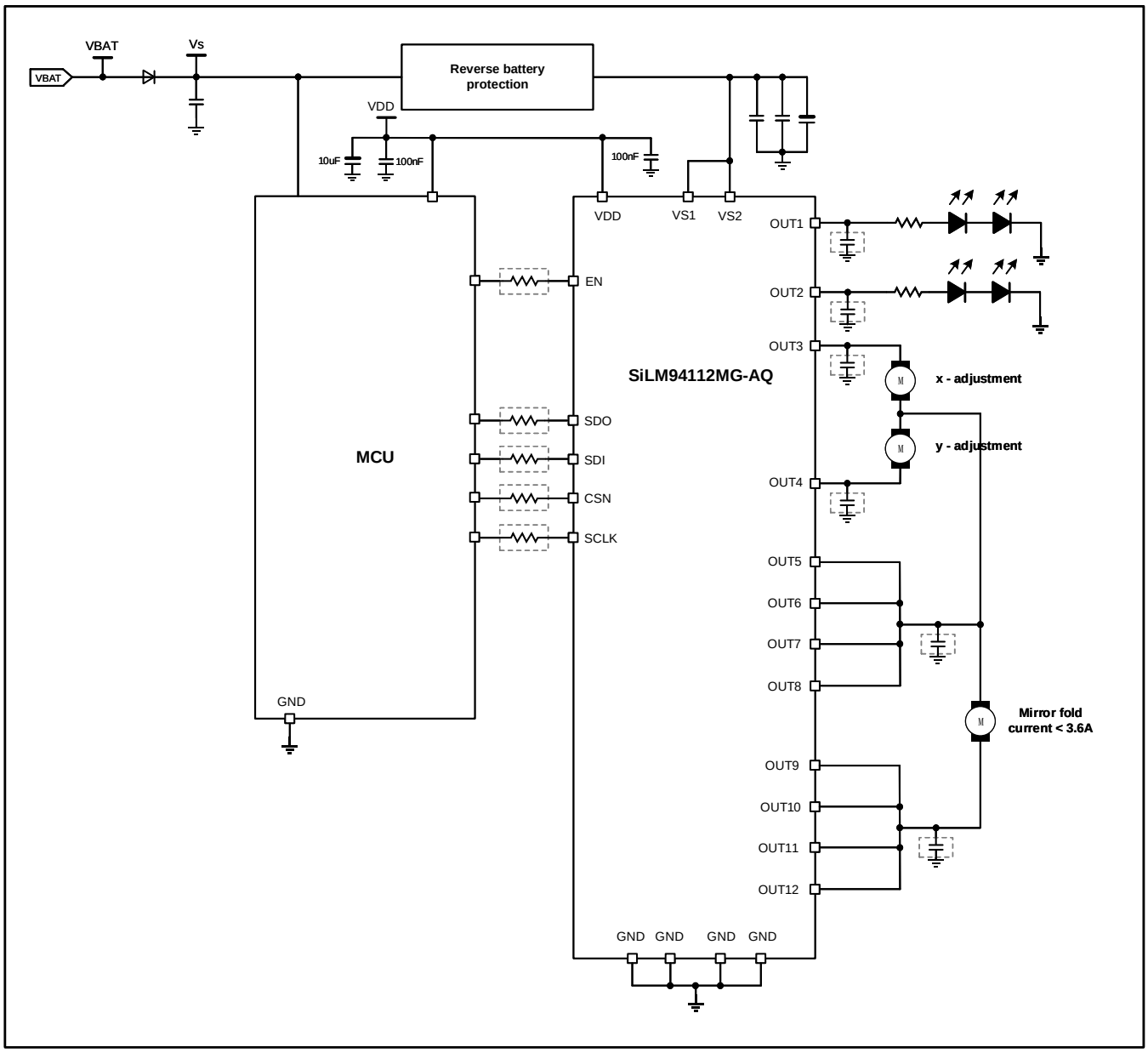
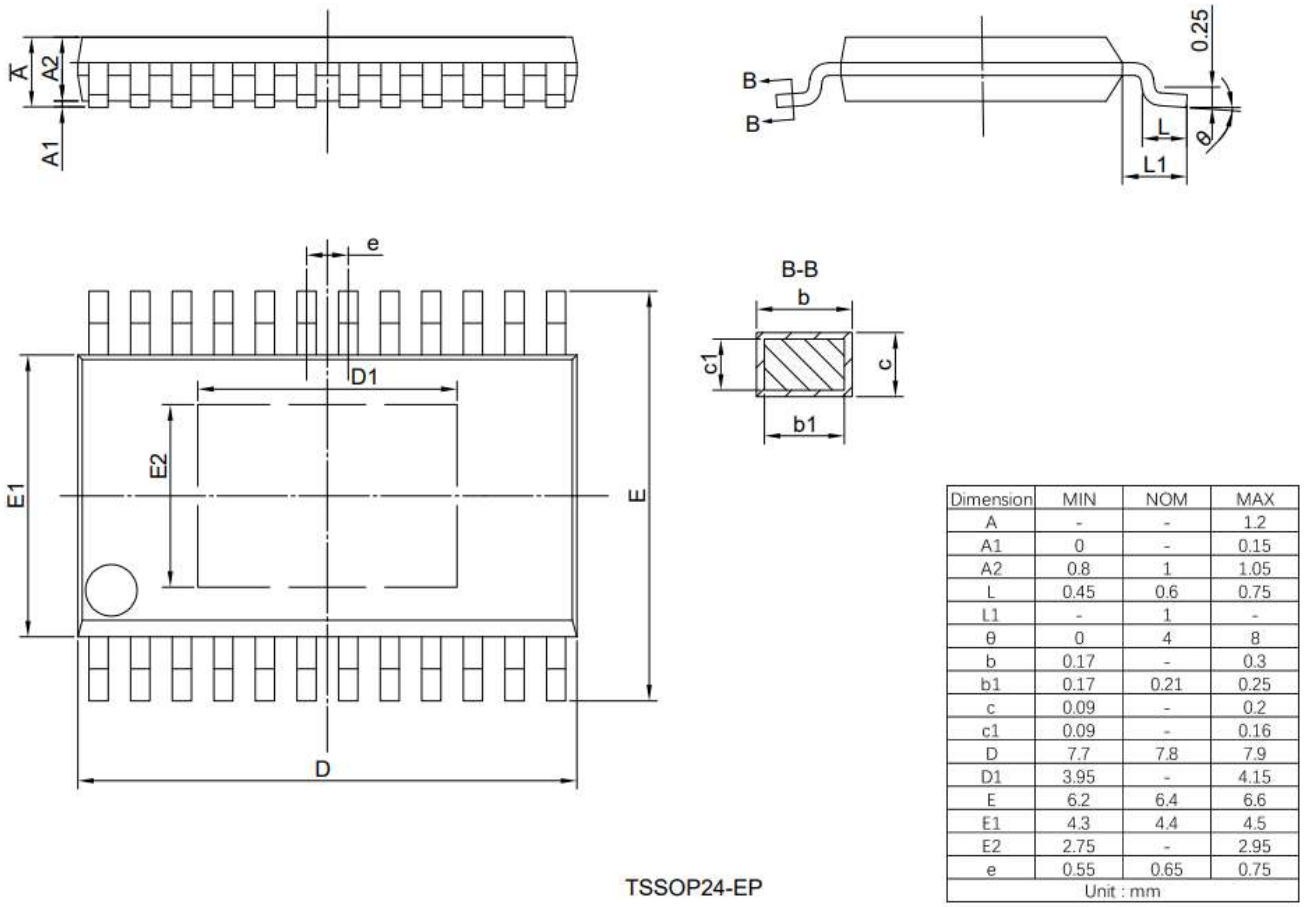


Figure 26. Application example for side mirror control

PACKAGE CASE OUTLINES



TSSOP24-EP

Dimension	MIN	NOM	MAX
A	-	-	1.2
A1	0	-	0.15
A2	0.8	1	1.05
L	0.45	0.6	0.75
L1	-	1	-
θ	0	4	8
b	0.17	-	0.3
b1	0.17	0.21	0.25
c	0.09	-	0.2
c1	0.09	-	0.16
D	7.7	7.8	7.9
D1	3.95	-	4.15
E	6.2	6.4	6.6
E1	4.3	4.4	4.5
E2	2.75	-	2.95
e	0.55	0.65	0.75
Unit : mm			

Figure 27. TSSOP24-EP Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2023-09-22	
Whole page	Initial released
Rev 1.1 datasheet, 2024-08-06	
Page 8	Add V_{ESD} HBM CDM Min Value
Page 9	Add I_{DD_Q} and I_{SQ} Max Value
Page 18	Update Figure 5, Figure 6
Page 20, 21	Previous status revised to New status in Figure 7, Figure 8
Page 56	Update Figure 26